Evaluating Monotone Circuits

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Joint work with

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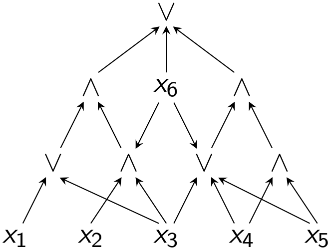
Circuits

A boolean circuit is a Directed Acyclic Graph (DAG), with each vertex(gate) is of the type AND,OR, and NOT, with a special vertex of fanout 0, called *root*.



Size : Number of non-input gates in the circuit.

Depth : Length of the longest directed path in the circuit.

Circuit Value Problem(CVP)

Given a Boolean circuit C_n and inputs $x_1, x_2, ..., x_n$. Decide whether $C_n(x_1, x_2, ..., x_n) = 1$ or not.

The General Version Captures Efficient Serial Computation

- P - Class of problems which can be solved by turing machines in time polynomial in the input length.
- Every problem in P has polynomial size circuit (family) which evaluate to 1 if and only if the corresp. Turing machine accept.
- General CVP is as hard as any problem in P . [Ladner, 1975]

Restricted CVP Captures Parallel Computation

Restriction : Depth is $\log^k n$, where n is the number of inputs.

- Efficient Parallel Computation : Polynomial number of processors running in poly-logarithmic time.
- Equivalent circuit characterisation : Polynomial size and poly-logarithmic depth (NC).
- CVP for this restricted class of circuits captures efficient parallel computation.

- Are there problems which have efficient serial algorithms but doesn't have efficient parallel algorithms? (Is $P \neq NC$?)

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Known in the monotone world !

Are there other natural restrictions that are easier ?

Monotone CVP

- Disallow NOT gates.
- Not too much of a restriction : Any circuit can be converted into this form by applying De-Morgan's laws without much blow-up in size. (Goldschlager 77)

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Planar CVP

- Underlying undirected graph should be planar.
- Planar : Embeddable in a plane with no edge crossings.
- Not too much of a restriction : There are gadgets which can replace crossings in a planar way.(Goldschlager 77)

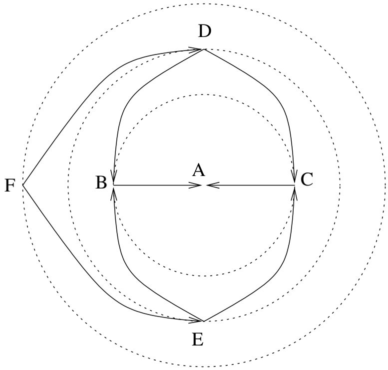
Planarity and Cylindricality

Input given as a combinatorial embedding ; the order of the edges from/to each of the vertices.

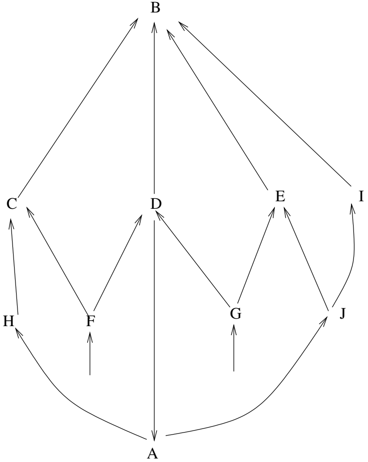
- Upward-Planar: There is a planar embedding such that every edge goes in a direction which is strictly increasing in y co-ordinate.
- Cylindrical: There is an embedding on the surface of a cylinder without crossings of the edges such that every edge is directed towards the endpoints of the cylinder.
- Layered: There is a partition of the vertex sets $V = V_0, V_1 \ldots V_h$ such that all edges go from some layer V_i to the next layer V_{i+1}.

They are different !

Cylindrical
Not Upward-planar



Planar
Not Cylindrical

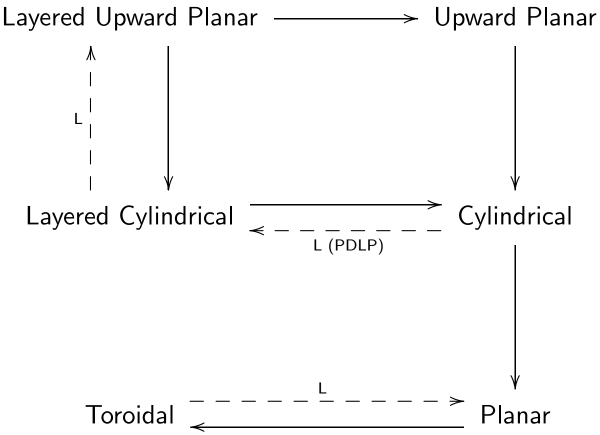


Mixing the two : Monotone-Planar CVP

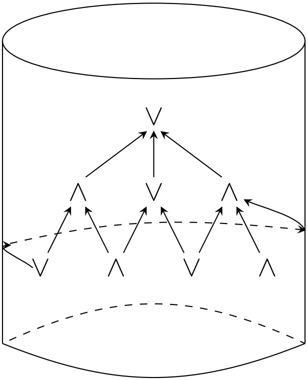
Given circuit is monotone and the underlying graph is planar.
Parallelizable : NC^3 algorithm (Yang 91).

- Upward Planar Layered Case, inputs in last layer : (Yang 91) gave an NC^2 algorithm. There were some recent improvements
- Upward Planar Layered Case (DK 93): log-depth parallel algorithms with queries to the above case.
  This gives an NC^3 algorithm.

Versions of Monotone circuits



From Layered Cylindrical to Layered Upward Circuits



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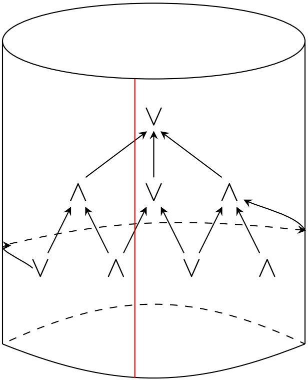

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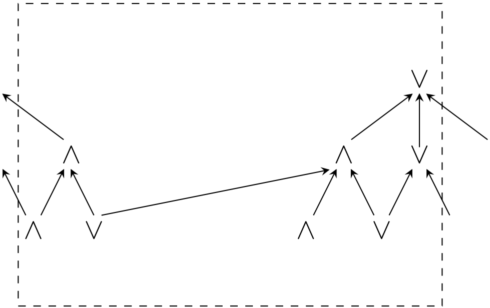

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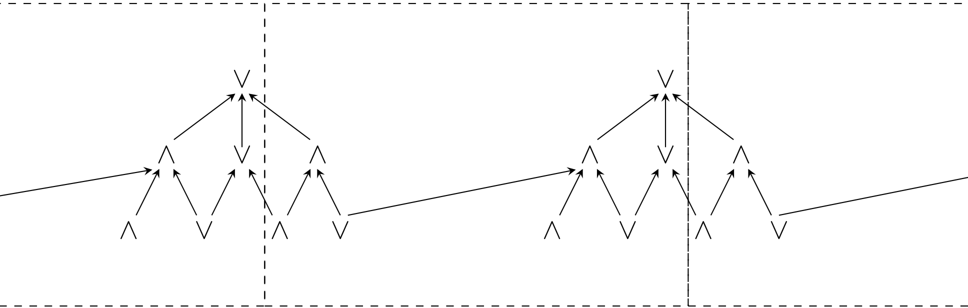


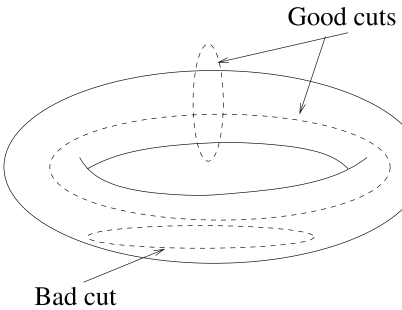
Claims..

- Let d be the depth of the circuit. Make d copies on either side and assign the dangling edges 0. The root of the copy at the center one is not corrupted.
- Finding the cut and patching up the copies can be done using only Log space.

Theorem

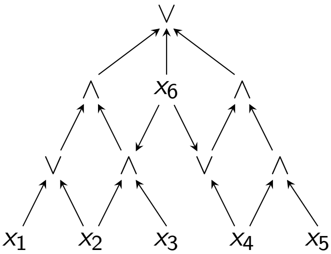
Given a circuit C of size s with a layered cylindrical embedding E, we can in log-space obtain an equivalent *circuit C_0 of size $(2d + 1)s$ with a layered upward planar embedding E'.*

From Toroidal to Planar



- Good cuts can be found in log space (ADR 05).
- Toroidal circuits can be converted to equivalent planar circuits.
- Evaluating Monotone Toroidal circuits in NC^3, but idea does not generalise.

Can we construct the layering ?



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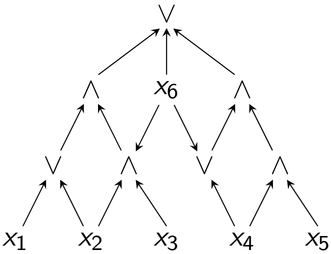
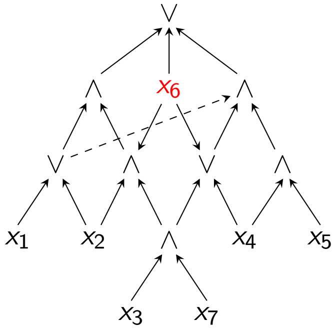


- Natural solution : Layer number of g is the length longest path to root from g (Yang 91).
- Suggests a log-space algorithm with queries to Longest-path.
- But this does not work when inputs are in many faces. There are counter examples.

Characterisation of Cylindrical Graphs

A graph G is *cylindrical* if and only if it is a *spanning subgraph* of a single-source single-sink planar graph H. (Hansen 03)
If G has only one *sink*, from a cylindrical embedding of G, the cylindrical embedding of H can be constructed in log space.



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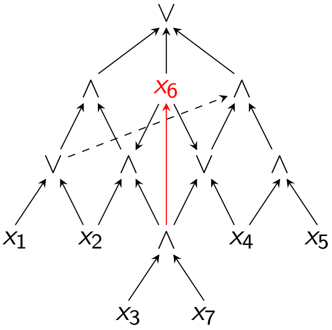


Layering cylindrical graphs

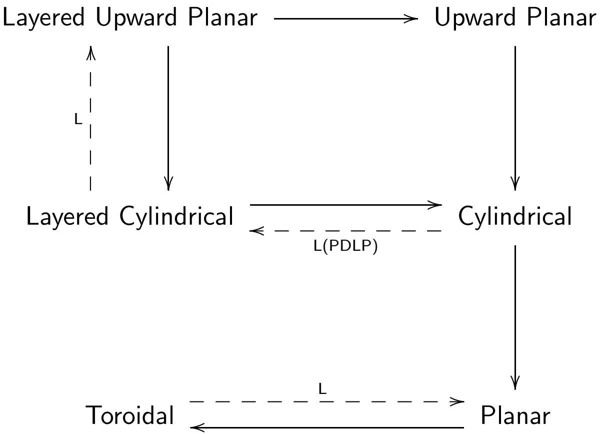
Algorithm to layer down the graph G is as follows,

- Eliminate all nodes which does not have a directed path to the root.
- Construct H and find its cylindrical embedding.
- Layer down H using the previous algorithm.
- Delete the extra edges added and patch to get the layered embedding of G.

Theorem

Converting a cylindrical circuit to an equivalent layered cylindrical circuit can be done in log-space with queries to Longest-Path.

Versions of Monotone circuits



Thank You