CS6868 - Concurrent Programming

Memory Consistency Models

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  - a contract between programmer and system.
  - Determines what optimizations can be performed for correct programs.
- Affects : Ease of programming, and performance

Uniprocessor Memory model

- Memory value requirement: Memory operations occur in program order: read returns the value of the last write in program order.
- Simple to reason about.
- Compiler optimizations preserve these semantics.
- Independent operations can execute in parallel.

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- Requires a Global clock $\equiv$ Halting problem.

Sequential consistency

[Lamport]: A multiprocessor system is sequentially consistent if the result of any execution is the same as if the operations of all processors were executed in some sequential order, and the operations of each individual processor appear in the order specified by the program.

Sequential consistency

Result of an execution appears as if:

- All operations executed in some sequential order.
- Memory operations of each process in program order.
- Nothing specified about caches, write buffers.

Understanding Program Order. Dekker's Algorithm

Initially Flag1 = Flag2 = 0

P1	P2
Flag1 = 1	Flag2 = 1
if (Flag2 == 0)	if (Flag1 == 0)
critical section	*critical section*

Execution:

P1	P2
(Operation, Location, Value)	*(Operation, Location, Value)*
Write, Flag1, 1	Write, Flag2, 1
Read, Flag2, 0	Read, Flag1, ___

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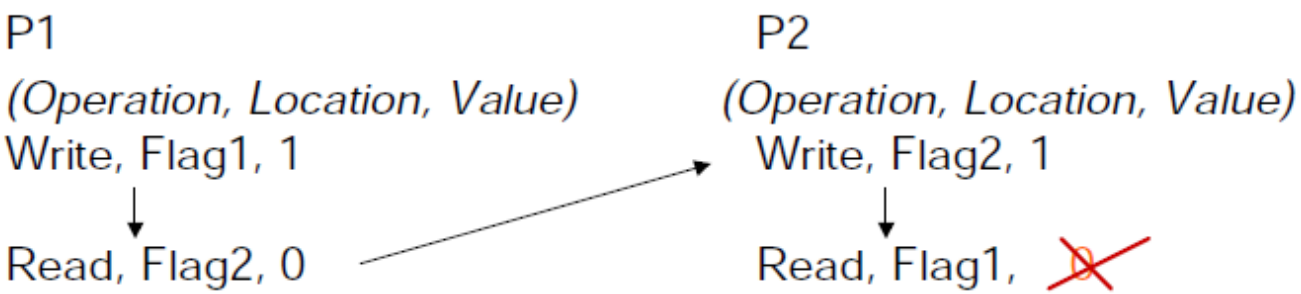

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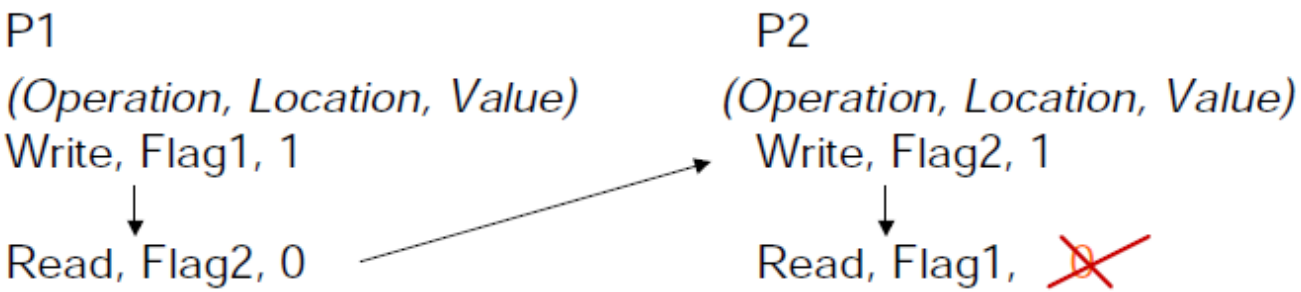

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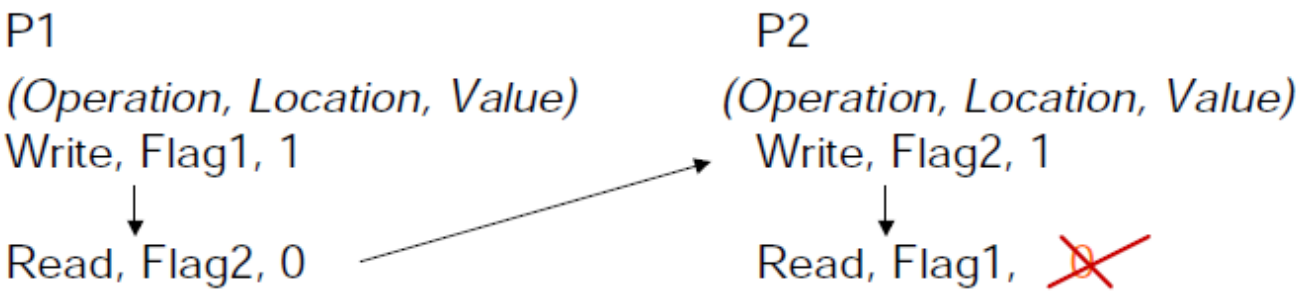

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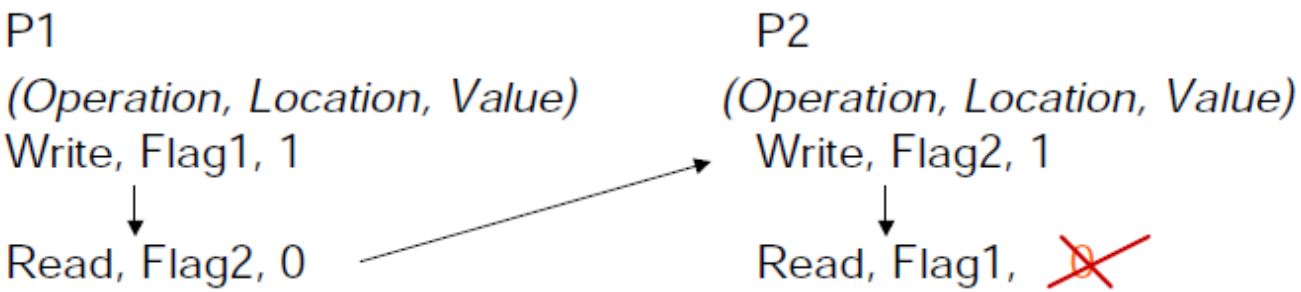

Reads of 1 by `Flag1 Flag2` are valid. Problematic situation

- Write buffers with read bypassing.
- Overlap or reorder writes/reads by compiler / hardware.
- Values in registers.

Understanding Program Order. Ex 2

Initially A = Flag = 0

P1
A = 23;
Flag = 1;

P2
while (Flag != 1) {;}
... = A;

P1
Write, A, 23
Write, Flag, 1

P2
Read, Flag, 0

Read, Flag, 1
Read, A, _____

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P2
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Problematic situation

- Overlap or reorder writes/reads by compiler / hardware.

Write Atomicity

Initially A = B = C = 0

P1	P2	P3	P4
A = 1;	A = 2;	while (B != 1) ;	while (B != 1) ;
B = 1;	C = 1;	while (C != 1) ;	while (C != 1) ;
		tmp1 = A;	tmp2 = A;

Q: What are the possible values of tmp1 and tmp2?

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- Cache coherence protocol must serialize writes to same location.
- Writes to same location should be seen in same order by all.

Atomicity Ex 2

Initially A = B = 0

P1	P2	P3
A = 1	while (A != 1) ;	while (B != 1) ;
	B = 1;	tmp = A

P1	P2	P3
Write, A, 1		
	Read, A, 1	
	Write, B, 1	
		Read, B, 1
		Read, A, ~~0~~

Atomicity Ex 2

Initially A = B = 0

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P1	P2	P3
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	Write, B, 1	
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- if ‘read’ returns a new value before all copies see it.

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- if 'read' returns a new value before all copies see it.
- Read others'-write early optimization is unsafe.

Sequential Consistency implementation

Implementations of this model must satisfy the following:

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- Program Order Requirement : The operations of same processor must be executed in program order
- Write Atomicity : All writes appear to be instantaneous (no buffer).
- All processors must see all write operations in the same order (cache coherence).
- Easier to implement in architectures with no cache, no write buffers, blocking reads, .

Sequential Consistency - issues

- Sequential Consistency constraints
  - write $\rightarrow$ read
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  - Processor reordering for performance - write buffers, overlapped writes, non-blocking reads
  - Compiler transformations - scalar replacement, register allocation, instruction scheduling.
  - Programmer reordering code for aesthetics/SE requirements.

Sequential consistency - too strict

- Many architectures do not give SC.
- Compiler optimizations on SC are limited.
- Sofwtware engineering issues.

- Give up!
- Use weaker models - relax the program order requirement and write atomicity requirement.

Sequential consistency (English)

- Memory operations of each process happens in program order.
- any valid interleaving of read and write operations is OK.
- all processes must see the same interleaving.

Sequential consistency examples

P1	W(x)1				
P2		W(x)2			
P3			R(x)2		R(x)1
P4				R(x)2	R(x)1

Sequentially consistent - as both P3 and P4 see writes in the same sequential order.

Sequential consistency (counter) example

P1	W(x)1				
P2		W(x)2			
P3			R(x)2		R(x)1
P4				R(x)1	R(x)2

Sequentially inconsistent - as both P3 and P4 see writes in the two different sequential orders.

Sequential consistency (counter) example

P1	P2	P3
x = 1;	y = 1	z = 1
print(y,z)	print (x,z)	print (x,y)

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x = 1;	y = 1	z = 1
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Inconsistent execution:

1. x = 1
2. print (y, z);
3. print (x, z);
4. y = 1;
5. z = 1;
6. print (x, y);

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  - program order for the ones issued by same processor.
- Hence such memory operations must be seen in same order by all processors.
- Here, write atomicity has been slightly weakened.
- weaker than sequential consistency, which requires that all nodes see all writes in the same order.

Causal consistency (example)

P1	W(x)1			W(x)3		
P2		R(x)1	W(x)2			
P3		R(x)1			R(x)3	R(x)2
P4		R(x)1		R(x)2	R(x)3	

Causally consistent, but not sequentially/strict consistent.

- Processors may see different order.
- All orders respect causal order (program order and read-write order).
- Has no global order, partial order for each processor.

Causal consistency (counter) Example

P1	W(x)1				
P2		R(x)1	W(x)2		
P3				R(x)2	R(x)1
P4				R(x)1	R(x)2

- Violates causal consistency.
- Removing the Read from the P2 – makes the execution causally consistent.

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- (Also known as, FIFO consistency, or Processor consistency)

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- Illusion of write atomicy has to be maintained.
- Hardware implementation of fence: processor has counter that is incremented when data op is issued, and decremented when data op is completed.

Weak Ordering

- Example 1:

P1	W(x)1 W(x)2 `Sync`	
P2		R(x)1 R(x)2 `Sync`
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- Example 2:

P1	W(x)1 W(x)2 `Sync`	
P2		`Sync`R(x)2

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P2		`Sync`R(x)2

- The programmer has to manage synchronization explicitly.
- Weak $\leq$ PRAM $\leq$ Causal $\leq$ SC $\leq$ Strict

Weak consistency (counter) example

P1 W(x)1 W(x)2 `Sync`

P2 `Sync`R(x)1

- P2 will observe the most recent write of the variable x, which has the value 2. Thus, it's not a valid sequence.

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- do “acquite” = that writes on other processors to protected variables will be known
- do “release” = that writes to protected variables are exported

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- A problem with weak consistency: when a synchronization variable is accessed, we do not know whether it is done because the process is finished writing shared data or is about to start reading data.
- Synchronization instructions divided : Acquire (such as lock) and Release (such as unlock).
- Acquire: Any memory operation after acquire must be executed only after acquire is completed (and seen by all).
- Release :
  - Release must be executed only when all memory operations statements are complete.
  - But accesses after ‘release’ in program order do not have to wait for release (unless protected by another acquire).
- do “acquite” = that writes on other processors to protected variables will be known
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- Total order among all synchronization instructions must be maintained.

Weak and Release comparison

- Weak: Shared data can be counted on to be consistent only after a synchronization is done.
- Release: Shared data are made consistent when a critical region is exited.

Release Consistency - example

- Example:

```
P1:   L W(x)1 W(x)2 U
P2:                     L R(x)2 U
P3:                                 R(x)1
```

- RC $\leq$ Weak $\leq$ PRAM $\leq$ Causal $\leq$ SC $\leq$ Strict

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  - if an object is modified, during the short period of time following its modification, the read may not be consistent.
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- **Eventual Consistency Model** : The writes propagates eventually (we cannot have a fixed bound on the delay)

Eventual Consistency

- Allow stale reads, but ensure that reads will eventually reflect previously written values (no guarantees on delays)
- Doesnt order concurrent writes as they are executed, which might create conflicts later: which write was first?
- More concurrency opportunities than strict, sequential, or causal consistency.
- Used a lot: Amazon: Dynamo, a key/value store, file synchronization

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  - How to reason about programs for systems with relaxed memory models
  - How to use the safety nets minimally, to get the desired semantics from program
- Even Sequential Consistency is not simple enough.
- We need models which is simple for the programmer, but provides enough information about program to apply optimization and get efficiency.

Programmer centric models

Programmers understand their code:

- Different operations have different semantics

P1	P2
A = 23;	while (Flag != 1) ;
B = 37;	. . . = B;
Flag = 1;	. . . = A;

- Flag = Synchronization; A, B = Data
- Can reorder data operations
- Distinguish data and synchronization

Data Race Free 0 - DRF0

- Data-Race-Free-0 Program
  - All access distinguished as either synchronization or data.
  - All races distinguished as synchronization (in any SC execution).
- Data-Race-Free-0 Model
  - Guarantees SC to data-race-free-0 programs.
  - Others - reads return value of some write to the location.

A program is considered to be data-race-free-0 if and only if (i) for any sequentially consistent execution, all conflicting accesses are ordered by the happens-before relation, and (ii) all synchronization operation in the program are recognizable by the hardware and each accesses exactly a single memory location.

Programming with Data Race Free 0 - DRF0

- Needed information: for each operation: if it will race (in any SC execution).
- Procedure:
  - Write program assuming SC.
  - For each memory operation in the program:
    - Guaranteed to be no races? “Data access”: “synchronization”.

Problems with data race free model

- It does not define any semantics for programs with data races.
- A concern for safe languages like Java, which provide safety for any program and cannot let the behavior of a program to be ambiguous.
- Either define safe semantics for such programs or identify them and prevent their execution.
- Define higher abstractions for programmers which are inherently data race free
- Expensive for hardware to implement

Goals of Memory model

- Programmability? - Lost intuitive interface of SC
- Portability? - Many different models
- Performance? - Can we do better?

Future:

- Parallel programs today are inherently non deterministic
- We need deterministic outcomes from our parallel programs.
- Deterministic Outcomes from Inherent non determinism. Possible?

Advantages from relaxed models

- Gains both in the H/W and compiler.
- Gains in H/W (during execution):
  - latency hiding - can overlap many reads and writes.
- Gain by the compiler:
  - more operations can be reordered. (compare with SC).
  -

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