**IITM-CS6840: Advanced Complexity Theory** Mar 15, 2012

# Lecture No. 39 : Circuit complexity classes

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THEME: Circuit Complexity Classes and their relationship to $\mathsf{L}$ and $\mathsf{NL}$
LECTURE PLAN:Define the NC and AC hierarchy and establish their relationship. Relationship between circuit complexity classes and space complexity classes.

We have already defined the following class.

$$\mathsf{NC} = \bigcup_{i \geq 0} \mathsf{NC}^i$$

where $\mathsf{NC}^i$ consists of those languages which have circuits over the basis $\{\wedge_2, \vee_2, \neg\}$ with logarithmic depth and polynomial size. We have also seen that $\mathsf{NC}^i \subseteq \mathsf{NC}^{i+1}$ for any $i$ and that $PARITY \in \mathsf{NC}^1$ and $ADDITION \in \mathsf{NC}^1$.

The class $\mathsf{NC}$ captures problems for which there are efficient parallel algorithms. It is an open question whether $\mathsf{P} \subseteq \mathsf{NC}$. That is, is every problem efficiently solvable in sequential machines efficiently solvable using parallel machines. Since $\mathsf{NC}$ is a non-uniform class it is not contained in $\mathsf{P}$.

**Claim 1.** $\mathsf{P} - UNIFORM - \mathsf{NC} \subseteq \mathsf{P}$

*Proof.* We first run the algorithm guaranteed by uniformity to generate the circuit. The we evaluate the circuit on the input to get the output. By the uniformity guarantee and the fact that $CVP \in \mathsf{P}$, we have the result. □

Similar to the notion of $\mathsf{NP}$-complete problems, we can define the notion of $\mathsf{P}$-complete problems. These are problems that are hard to parallelize. The most obvious candidate for a $\mathsf{P}$-complete problem is the $CVP$ problem. We know that any problem in $\mathsf{P}$ can be reduced to $CVP$ using a logspace reduction (We'll show that $\mathsf{L}$ is contained in $\mathsf{NC}$). So if $CVP$ is parallelizable, so is any problem in $\mathsf{P}$.

Let us think about circuits where gates are allowed to have unbounded fan-in. The concepts of fan-in and fan-out are the same as those in digital logic. We fix the basis as $\{\wedge_n, \vee_n, \neg\}$. It is easy to see that $ADDITION$ can be solved by a depth-3 circuit if unbounded fan-in is allowed. However, it is not at all clear whether we can compute $PARITY$ by constant depth circuits of polynomial size. We now define new classes to incorporate this new basis.

$$\begin{aligned} \mathsf{AC}^i &= \{L : L \text{ can be computed by depth } O(\log^i n) \text{ circuits of polynomial size}\} \\ \mathsf{AC} &= \bigcup_{i \geq 0} \mathsf{AC}^i \end{aligned}$$

**Claim 2.** $\mathsf{NC}^i \subseteq \mathsf{AC}^i \subseteq \mathsf{NC}^{i+1}$

*Proof.* The first inclusion holds trivially since any gate with bounded fan-in can be thought of as a gate with unbounded fan-in. Now we prove the second inclusion. Take any unbounded fan-in AND gate. Replace this unbounded fan-in gate by a balanced binary tree of bounded fan-in AND gates. Since the fan-in of the unbounded gate is at most polynomial (the circuit is polynomial size), the depth of the tree is at most $\log(n)$. This construction can be carried out for an unbounded OR gate. So the circuit depth increases by at most a logarithmic factor. Thus the resulting circuit has depth at most $\log^{i+1}(n)$. □

It follows that $\mathsf{NC} = \mathsf{AC}$. We now show that these complexity classes defined in terms of circuits are related to the space complexity classes $\mathsf{L}$ and $\mathsf{NL}$.

**Theorem 3.** $\mathsf{NL} \subseteq \mathsf{AC}^1$

*Proof.* We use proof for Savitch's theorem. Remember that the reachability problem for directed graphs is $\mathsf{NL}$-complete. For each vertex pair $(u, v)$ and distance $2^k$ where $0 \leq k \leq 2 \log n$, we will implement a circuit computing the reachability predicate "Is $v$ reachable from $u$ in $2^k$ steps"?. When $k = 0$, this amounts to checking the corresponding bit in the adjacency matrix and can be implemented by a trivial circuit. Now assume that the circuits for $k - 1$ are available (there are $n^2$ of them). We can construct a circuit for $(u, v, 2^k)$ by taking the OR over all $(u, w, 2^{k-1})$ *and* $(w, v, 2^{k-1})$ for all intermediate vertices $w$. Note that the depth of the circuit is $O(k) = O(\log n)$ and size of the circuit is $O(k.n^2) = O(n^2 \log n)$. □

**Theorem 4.** $\mathsf{L} - UNIFORM - \mathsf{NC}^1 \subseteq \mathsf{L}$

*Proof.* First use the $\mathsf{L}$-uniformity to generate the appropriate circuit. Since it is an $\mathsf{NC}^1$ circuit the depth is at most $\log n$. Doing a DFS on this circuit takes only logarithmic space. We know that circuit can be evaluated by a DFS. □

The above proof doesn't work for $\mathsf{L} - UNIFORM - \mathsf{AC}^1$ since the gates could be of unbounded fan-in. So to keep track of the path to backtrack we have to spend $\log n$ bits per each level and therefore $\log^2$ space in total. So we have $\mathsf{L} - UNIFORM - \mathsf{AC}^1 \subseteq \mathsf{DSPACE}(\log^2)$.

We know that $AND$ can be computed by an $\mathsf{AC}^0$ circuit. It is easy to see that $\mathsf{NC}^0$ cannot contain $AND$. This is because constant depth circuits with bounded fan-in gates cannot implement functions that depend on all its input bits. However, the function $AND$ depends on all input bits. We'll show later in the course that $\mathsf{AC}^0$ is properly contained in $\mathsf{NC}^1$ by showing that to implement $PARITY$ using a constant-depth circuit requires an super-polynomial size.