Jyothi Krishna V S

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Research Interests

Concurrent Programming, Compiler Design and Optimization for Parallel Programs, Compiler Design for Heterogeneous Architectures, Parallel Program Analysis.

Education

- **PhD** — IIT Madras, Chennai
  CSE: Compiler Optimizations for Asymmetric Multicore Processors — *CGPA 9.25, July 2013-*
- **MTech** — IIT Madras, Chennai
  Computer Science and Engineering — *CGPA 8.88, 2009-2011*
- **BTech** — CET, Thiruvananthapuram
  Computer Science and Engineering — *CGPA 7.43, 2005-2009*

Work Experience

- **Adobe Systems India Pvt Ltd.** — Bangalore.
  Member of Technical Staff — *July, 2011 - July, 2013*

Papers and Publications

- Journal:*CHOAMP:Cost Based Hardware Optimization for Asymmetric Multicore Processors*, Jyothi Krishna V S, Shankar Balachandran, Rupesh Nasre. Submitted to IEEE Transactions on Multi-Scale Computing Systems (TMSCS).
- Workshop Paper:*Identifying Use-After-Free Variables in Fire-and-Forget Tasks*, Jyothi Krishna V S and Vassily Litvinov, in Chapel Implementers and Users Workshop (CHUIW), Jun '17.
- Workshop Paper:*Compiler Enhanced Scheduling For Heterogeneous Multicore Processors*, Jyothi Krishna V S and Shankar Balachandran, in 2^{nd} Energy Efficiency with Heterogeneous Computing (EECHO) Workshop, Jan '16.
- Student Poster:*OpenMP Compiler For Heterogeneous Multicore Processors*, Jyothi Krishna V S and Shankar Balachandran, Poster at European Network on High Performance and Embedded Architecture and Compilation (HiPEAC), Jan '16.
- Patent Applied:*3293US01 - Application - US - 14/020,579 Device Context-based User Interface*. Anand Samuel Edwin, Charan Raj, Rahul Kumar Agrawal, Senthilkumar PanneerSelvam, Jyothi Krishna V S .

Attended Conferences and Workshops

- Attended IEEE International Parallel and Distributed Processing Symposium (IPDPS '17) held at Florida, May 29- Jun 02, 2017.
- Attended European Network on High Performance and Embedded Architecture and Compilation (HiPEAC '16) held at Prague, Jan 18-20, 2016.

Last modified : April 19, 2018

- Attended Annual Symposium on Principles of Programming Languages (POPL '15) held at Mumbai, Jan 12-18, 2015.

Projects

- **PhD Thesis**
  - CHOAMP, A Cost Based Hardware Optimization for Asymmetric Multicore Processors: Using regression techniques, with the help of an Oracle trained offline for the target Asymmetric hardware and compile time analysis of task workload in a parallel program, to find the optimal hardware configuration to run the program.
  - CES, Compiler Enhanced Scheduling for OpenMP programs for Heterogeneous Multicore Architecture: Compiler analysis and transformation for optimizing on the run-time of a parallel program in an Asymmetric Multicore environment.
- Chapel Compiler: Writing compiler passes for identifying possible access of freed variable that would result in incorrect execution of the program. We have developed a pass in Chapel compiler to identify and report such variable uses. The Developed pass is yet to be merged with Chapel mainline.
- AUTOPAR for OpenMP: Identifying and transforming sequential loops that can be parallelized using additional Barriers in OpenMP using ROSE framework. We were able to identify non parallel loops with dependencies and introduce barrier to handle these dependencies and convert it to parallel loops. Done as a part of Course Project.
- Static Race Detection And Scalability Analysis Of X10 Programs: A Cilk View (for predicting the effective speed-up) and Cilk Screen (for identifying race conditions) inspired compile-time tools for X10. X10-View was able to identify the effective parallelism for different number of hardware threads available. The results were quite different from the run-time behaviours due to the varying cost of synchronization constraints. Done as a part of Course Project.
- Sequential Program Scheduler: Efficiently scheduling sequential programs while being run simultaneously with parallel programs with variable thread workload. Done as a part of Course Project.
- (**MTech Project**) Probabilistic circuits generation: Automating the Generation of efficient Probabilistic Circuits for a given set of outputs and minimization of the generated probabilistic circuits. We were able to automate the probabilistic circuit construction with the given accuracy.
- (**BTech Project**) Automated Robotic Mapper: An intelligent robot which could find the obstacles in front of it and provide its distance and size and shape to a remote computer to help mapping the area. Used Audrino board for controlling the robot and Infrared signals from a remote server to communicate with it.