Emerging Computational Devices, Architectures and Computational Models

Overview

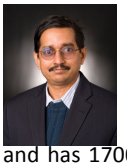
As traditional CMOS scaling nears the end of physical scaling, the need for new computational devices, models and architectures has become imperative. At the application-level the systems are evolving from number-crunching compute modules to intelligent systems capable of cognitive thinking. This short course will look at the synergies that are required across the stack from new devices to new computational models for designing future computing systems. As physical dimensional scaling alone has ceased to be the key factor driving the industry, many innovations have occurred in designing new types of switches including changes to their structure (such as three-dimensional Finfets), their underlying physics (use of tunneling for steep-switching devices), the material systems (integration of ferro-electrics in gate stack for Negative Capacitance FETs). The first part of the lecture will introduce these devices and accompanying circuit innovations.

There has been a world of revolution in the memory devices with the emergence of many non-volatile memory devices and their tight integration in cross-point architectures. These memory systems have enabled new styles of computing systems such as the non-volatile processor for Internet of thing systems and neuromorphic computing systems for cognitive computing. The lectures will focus on the synergistic coordination in advances in devices to system design. Another emerging novel computational model is based on the principle "let physics do the computation". This technique focuses on using the intrinsic operation mechanism of devices (such as nanoscale electronic coupled oscillators) to do the computation, instead of building complex circuits to carry out the same function.

This course will introduce the following topics: Emerging logic and memory devices; Circuit/Architecture design using Emerging Logic and Memory devices; Processor-in-Memory Architectures using emerging devices; Neuromorphic and Brain-Inspired Computational Models; Computing Using Coupled Oscillator Systems; and Other Emerging Computational Models.

Dates for the Course	**11th December, 2017 to 15th December, 2017**
Host Institute	**IIT Madras**
No. of Credits	**1**
Maximum No. of Participants	**50**
You Should Attend If…	▪ You are an electronics or computer science engineer or research scientist interested in exploring emerging logic and memory technologies as well as computational models. ▪ You are a student or faculty from academic institution interested in exploring new computational paradigms beyond Von-Neumann computing models.
Course Registration Fees	The participation fees for taking the course is as follows: **Participants from Abroad:** US$ 500 **Participants from Industry/Research Organizations:** Rs. 20,000 **Participants from Academic Institutions**: Rs. 5,000 **Students from IIT Madras:** Free **Students from other Recognized Academic Institutions:** Rs.1,000 The above fee is towards participation in the course, the course material, computer use for tutorials and assignments, and laboratory equipment usage charges. **Mode of payment: Demand draft in favour of "Registrar, IIT Madras" payable at Chennai** The demand draft is to be sent to the Course Coordinator at the address given below.
Accommodation	The participants may be provided with hostel accommodation, depending on the availability, on payment basis. Request for hostel accommodation may be submitted through the link: http://hosteldine.iitm.ac.in/iitmhostel

Course Faculty



Prof. Vijaykrishnan Narayanan is a Distinguished Professor of Computer Science and Engineering and Electrical Engineering at The Pennsylvania State University. He has more than 400-refereed publications and has 17000+ citations to his work with an h-index of 68. He is a Fellow of IEEE and ACM. He has won several awards in recognition of his research including the IEEE Micro Top Picks for 2016, ASPDAC ten-year retrospective most influential paper award, IEEE Transactions on VLSI Best Paper Award, One of the most significant papers of FPL in the 25-year history of Conference. He is listed in the Hall of Fame of the top computer architecture conferences: ISCA and HPCA. He also owns multiple patents on architectures for emerging technologies and applications. He has provided invited technical briefing at the US Senate and invited demonstration at the Science Fair at the US Congress. He has also been an invited attendee at the White House Brain Conference. His work has been widely featured in technical press.

Prof. Narayanan leads an internationally renowned National Science Foundations (NSF) expeditions-in-computing center and is an investigator of three other major multi-university centers: DARPA/SRC LEAST Center, NSF ERC ASSIST and NSF/SRC E2CDA centers.

Prof. Narayanan has provided several lectures and short courses to institutions around India as part of the Indo-US Collaboration on Engineering Education. He is currently the Editor-in-Chief of IEEE Transactions on Computer Aided Design, the Chair of the ACM Special Interest Group on Design Automation and also served as the founding co-editor-in-chief of the ACM Journal of Emerging Technologies in Computing Systems.

Prof. V. Kamakoti is a professor in the Department of Computer Science and Engineering, IIT Madras. His research interests include Software for VLSI, Reconfigurable Systems Design and Computer Architecture.

Prof. Madhu Mutyam is a professor in the Department of Computer Science and Engineering, IIT Madras. His research interests include multicore architecture, memory system design and network-on-chip.

Course Coordinators

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