Pritam Majumder
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Objective: I am open to explore and research any aspects in Computer Architecture**.** Currently I am working on pipelined data cache memory to reduce its per-access energy consumption and also improve its access latency.

Publication (s):

Pritam Majumder, Venkata Kalyan T, Madhu Mutyam, *SFFMap: Set-First Fill Mapping for an Energy Efficient Pipelined Data Cache,* IEEE International Conference on Computer Design (**ICCD**) 2014, pp.104-109.

Current Research Interest:

MS Thesis Guide: Dr. Madhu Mutyam (Associate Professor, CSE Dept., IIT Madras)

- **Major Project:**

  Cache Memory Energy Optimization and Performance Improvement: Since on-chip caches consume almost one-third of the processor energy, has been a concern for chip design architects for a since late ninetieth century. There are a significant number of works in literature that address this energy consumption issue and propose several energy efficient cache designs. Our focus is on data cache energy optimization. We propose to utilize the last stage of the pipeline registers as a set-buffer, and service the data requests of the processor from this set-buffer if consecutive requests are to the same set. Instead of using all the pipeline stages of the data cache, on every data cache access, data can be supplied from the last pipeline stage itself, saving the access energy of first three pipeline stages. Moreover, since this also reduces the access latency of the data cache whenever there is a set-buffer hit, overall performance is also improved. On an average we have achieved 27% energy savings and 5% performance improvement from a conventional data cache system. We have conducted all the experiment using **Gem5** simulator and estimated the circuit's energy consumption and area requirement using **Cacti-6.5** simulator.

- **Minor Project (s):**

  - **Data Prefetching:** Implemented a feedback directed stream prefetcher and a timely prefetcher and compared the performance with normal stride prefetcher and a delta-correlation prefetcher for both single core and multicore system, with Network On Chip (NOC), using **Multi2Sim** simulator.

  - **Cache Replacement Policy:** Implemented and compared different replacement policies at the presence of a stride and delta-correlation prefetcher to observe the performance dependence of the prefetcher on different replacement policies.

  - **Modeling Simple Scalar and Super-Scalar Processor:** Both are designed and modeled using Verilog HDL.

  - **Hands-on FPGA board:** A small code detection project is implemented on FPGA board, where input code was fed by UART and at the output, the input code is reversed and shown using the on-board LED(s).

Education:

University/ Board	Qualification/ Degree	Institute	Year of Passing	CGPA/%
IIT Madras	MS	IIT Madras	2015 (expected)	8
WBUT	B.Tech	CIEM	2011	8.63
WBCHSE	Higher Secondary	B.T.Rd. Govt. Spons. H.S. School	2007	86%
WBBSE	Secondary	B.T.Rd. Govt. Spons. H.S. School	2005	90%

Advance Courses Attended (related to the research field):

- Advance Computer Architecture, CAD for VLSI, Parallel Computer Architecture, Digital Design Verification.

Undergrad Project (s) and Publication (s):

(1) D. Ghosh, **Pritam Majumder** and A. Kumar Das, *Intelligent Energy Efficient Routing for Ad-Hoc Sensor Network by Designing QCS Protocol*, 4th International Conference, CNSA 2011, Chennai, India.

(2) D. Ghosh, **Pritam Majumder** and A. Kumar Das, *A New Energy Efficient Approach Towards WASN Routing with Modified QCS Protocol*, IJASUS, 2011

(3) **Photo Gallery Project:** Designed and built a photo gallery website as part of summer project in 3rd year of Undergrad.

Teaching Experience:

(1) Teaching Assistant in CS1100, Computational Engineering (Jan'12 - May'12).
(2) Teaching Assistant in CS4100, Computer System Design (July'12 - Nov'12).
(3) Teaching Assistant in CS1100, Computational Engineering (Jan'13 - May'13).
(4) Teaching Assistant in CS4100, Computer System Design (July'13 - Nov'13).
(5) Teaching Assistant in CS6560, Parallel Computer Architecture (Jan'14 - May'14).
(6) Teaching Assistant in CS1100, Computational Engineering (July'14 - Nov'14).

Award (s):

(1) Outstanding Teaching Assistantship award in 2012, CSE, IIT Madras
(2) Outstanding Teaching Assistantship award in 2013, CSE, IIT Madras
(3) India Government Scholarship (for obtaining rank 62 in the 10th State Board Exam) in 2005

Technical Skill (s):

(1) Extensively modified Gem5 simulator for designing required hardware components using **C++**.
(2) Designed a small data base system using **C** language. Used **C** to model various components in Multi2Sim simulator.
(3) Designed and realized a simple-scalar and a super-scalar processor using **Verilog**.
(4) Synthesized few hardware components after designing in Verilog using **Xilinx ISE**.
(5) Validated undergrad project in **MATLAB.**
(6) Designed and built photo gallery website using **JSP**.
(7) Apart form the afore mentioned skills enough obtained exposure in - **JAVA**.

Reference (s):

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