CS 2310 – Digital Logic And Design Laboratory

L-T-P-C: 0 - 0 - 3 - 1

1. Design AND, OR and EX_ OR gates using Nand (7400) gates and verify them.

2. (A) Design a BCD to 6-3-1-1 Code converter and verify.

   (B) Design a 6-3-1-1 to Gray Code converter and verify.

3. Design a full adder circuit using AND, OR and XOR gates. Verify it.

4. Design a 4 – Bit comparator using logic gates.

5. Design a Pseudo-random bit generator and check its performance.

6. Design a 4 – bit ripple carry adder, and verify by adding unsigned and signed integers. Check the overflow condition. Use BCD-to-SSD Decoders to demonstrate the results.

7. Design a Master – Slave J-K Flip-Flop using Logic gates.

8. (A) Design a Bi - directional counter using J-K Flip-flops.

   (B) Design a Counter which counts the following arbitrary sequence: 0101, 0001, 1000, 1001, 1010, 0000, 0101…

9. Design a priority multiplexer for 8 Devices. Each device has one data output line, a request output line, and an acknowledgement input line. The data from the highest priority device has to be made available at the output of the priority multiplexer, and an acknowledgement has to be sent to that device.

   Hint: The circuit may be designed using priority encoder, multiplexer and decoder.

10. Write and verify a VHDL code, using verilog, for simulation of a 4- Bit fast look ahead carry adder using logic gates, full adders etc.

11. Write and verify a VHDL code, using verilog, for simulation of an 8-bit signed integer multiplier using carry save adders.