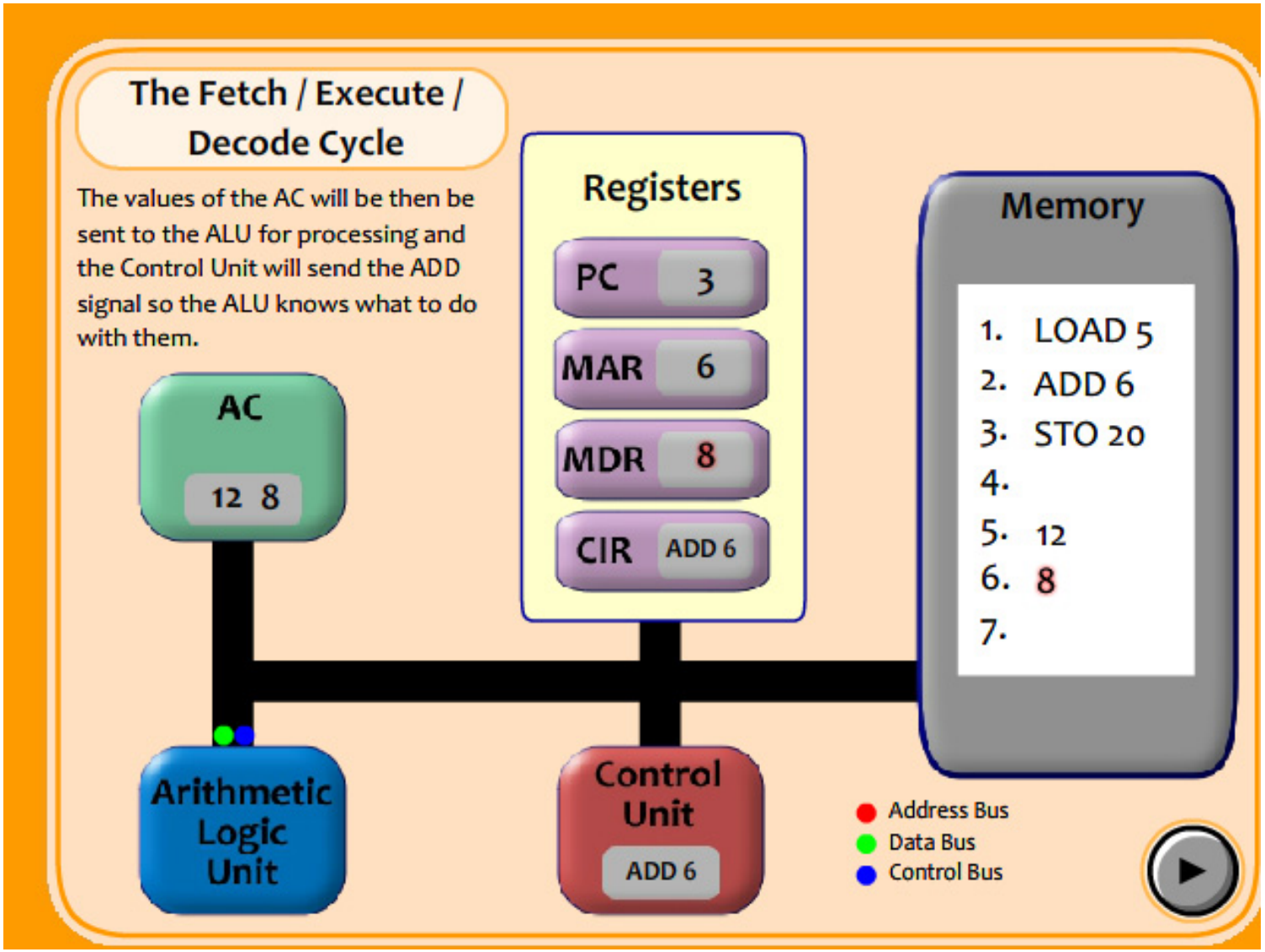
Basic Illustrations

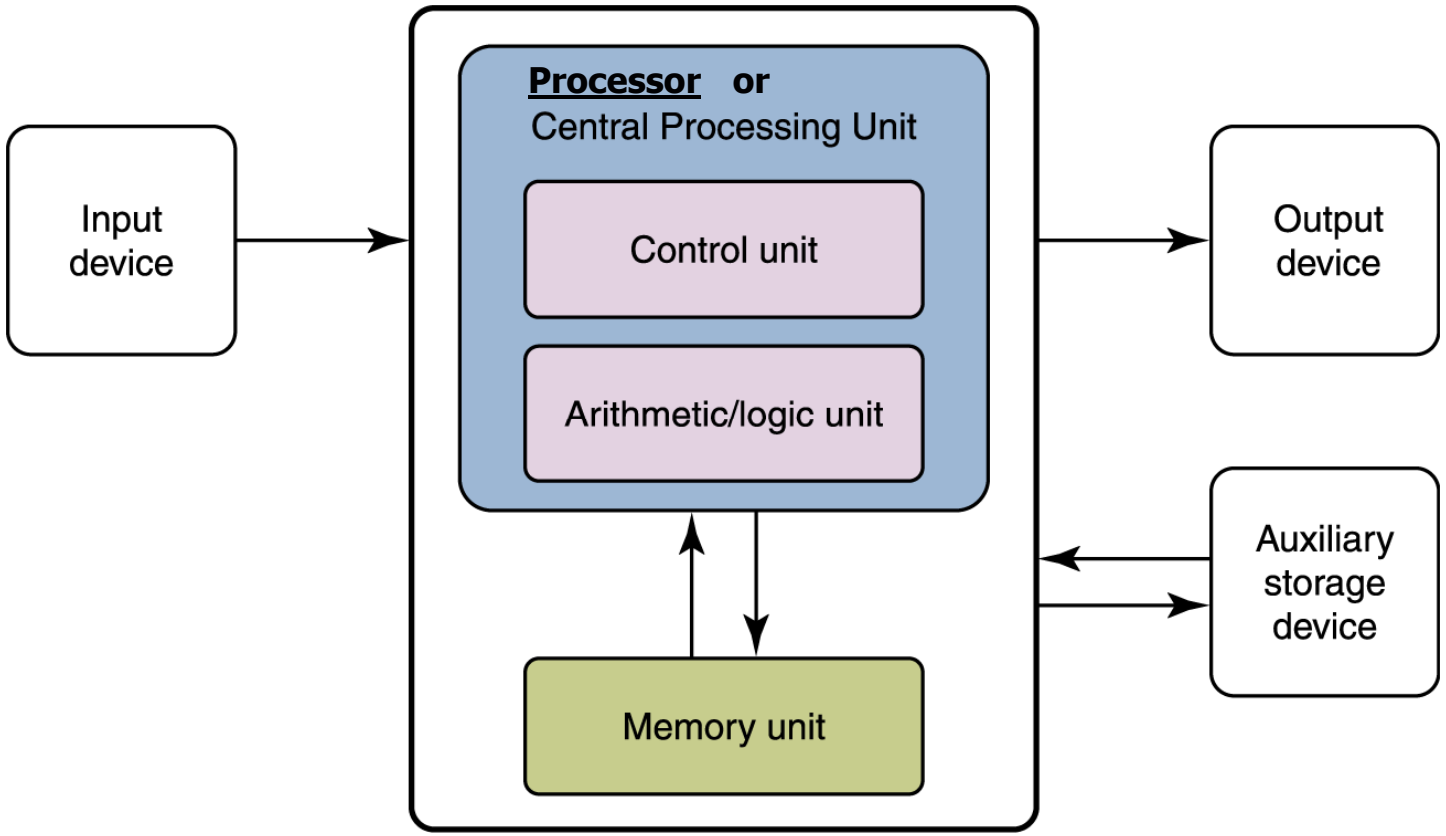
Functions/units of CPU;

Followed by logic gates.

www.hartismere.com/Subjects/ICT/ALevelComputing/CPUCycleAnimation

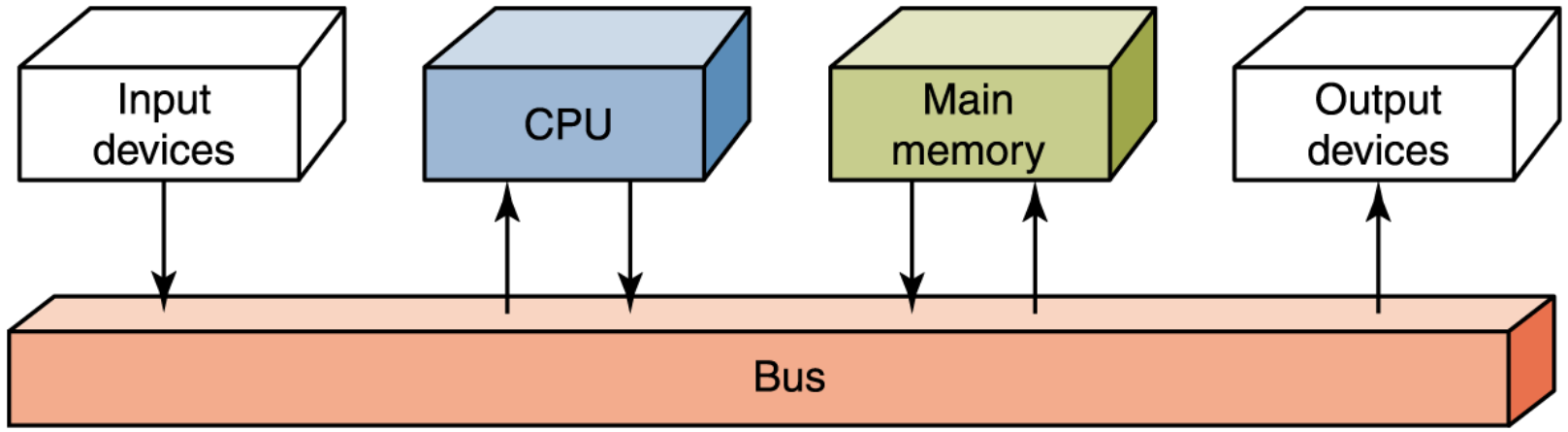


The von Neumann Architecture of a Computer



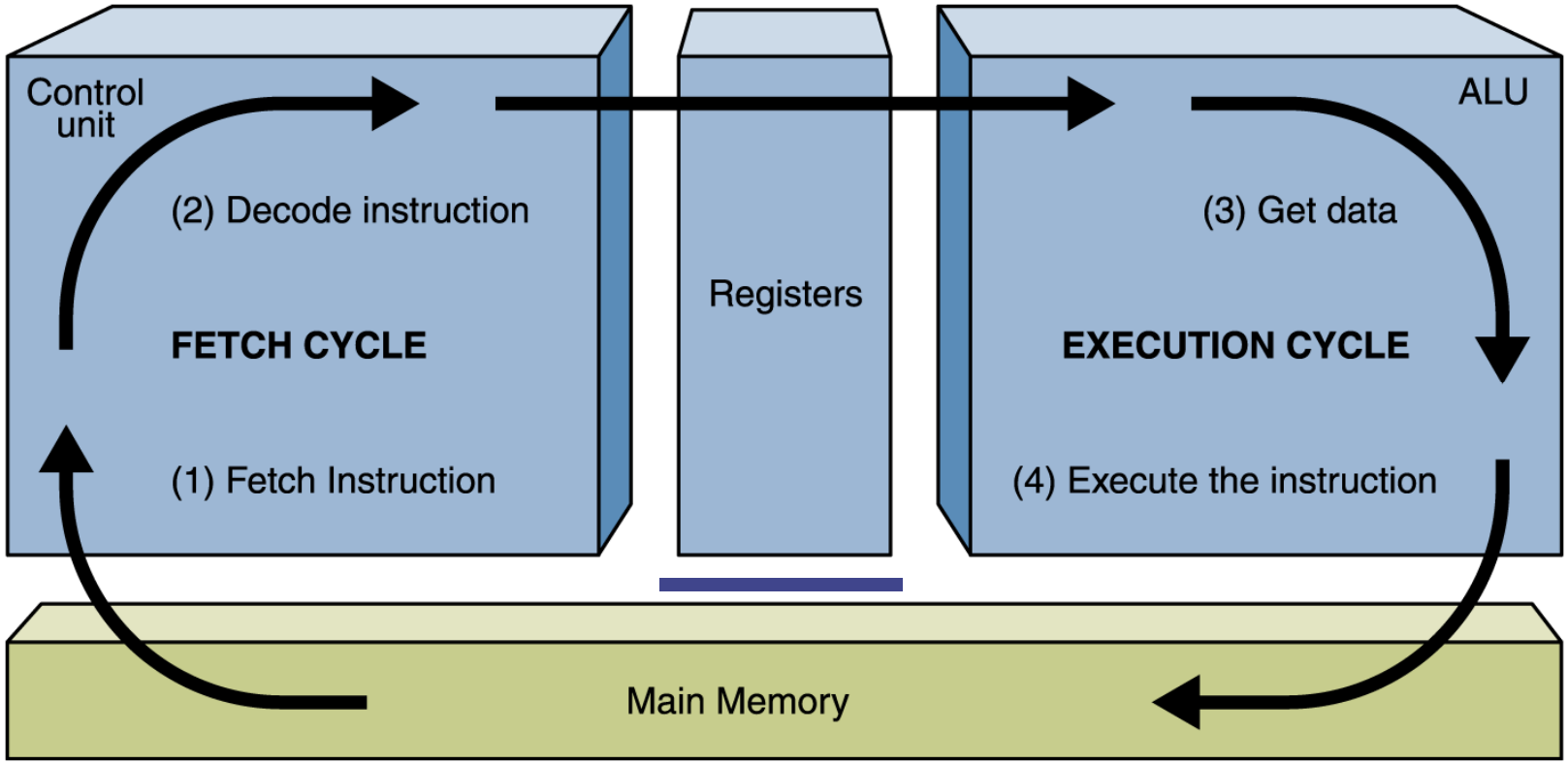
Simple single-bus architecture

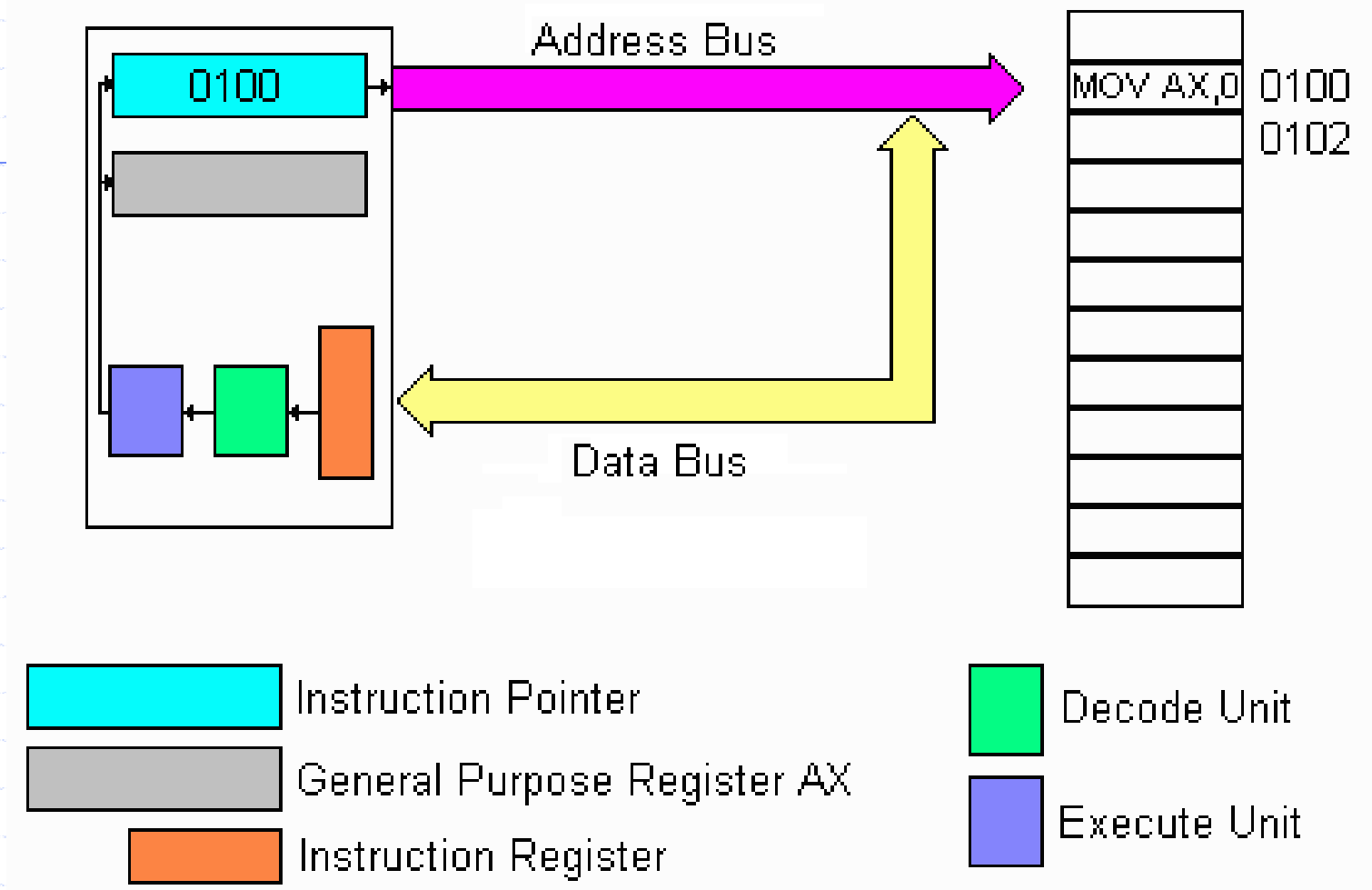
- The parts are inter-connected by a collection of wires called a "bus".

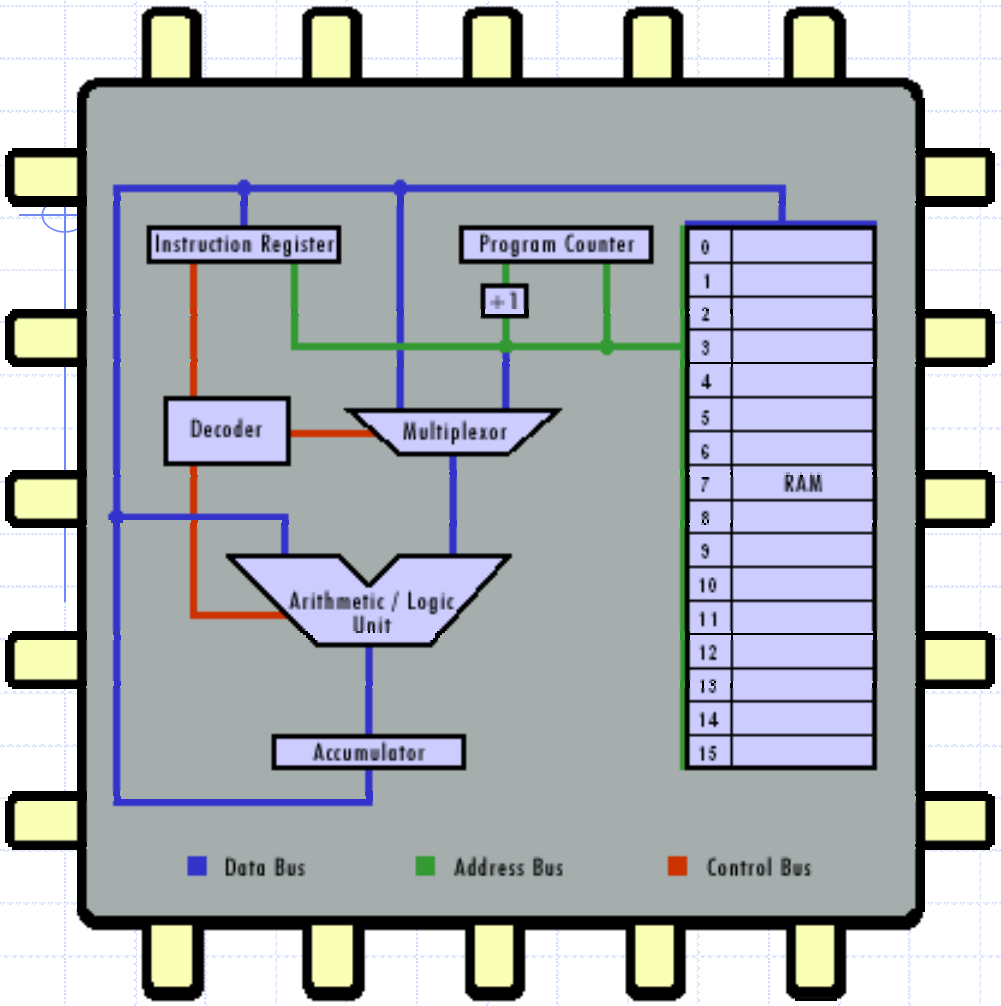


Data flow through a von Neumann architecture

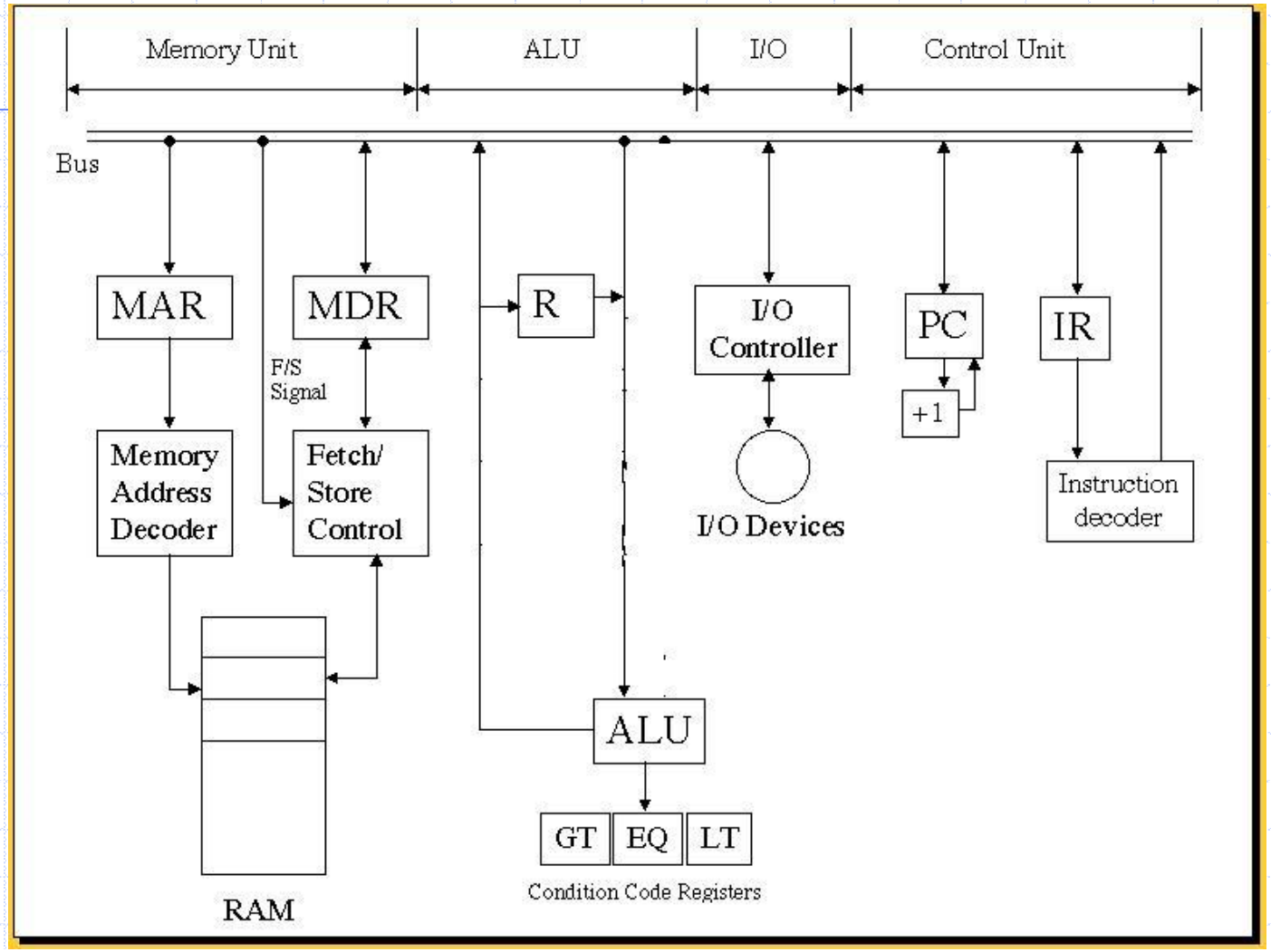
The Fetch-Execute Cycle

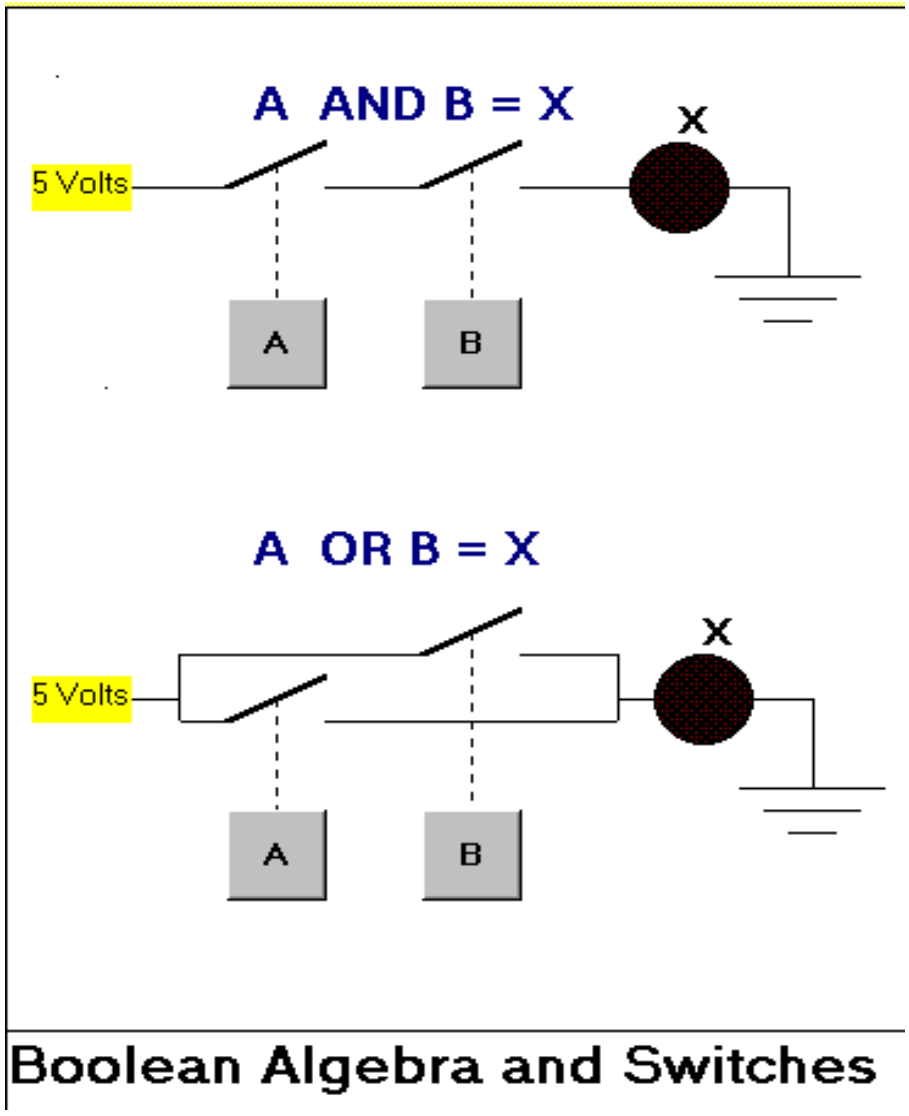



Address Bus
0100
MOV AX,0
0100
0102
Data Bus
Instruction Pointer
General Purpose Register AX
Instruction Register
Decode Unit
Execute Unit


Instruction Register
Program Counter
+1
Decoder
Multiplexor
Arithmetic / Logic Unit
Accumulator
0
1
2
3
4
5
6
7
RAM
8
9
10
11
12
13
14
15
Data Bus
Address Bus
Control Bus

A simple Computer Architecture





Boolean Algebra and Switches

Positive Logic		Negative Logic	
INV			INV
AND			OR
NAND			NOR
OR			AND
NOR			NAND

Categories in Digital System Design :

- System Level

- Logical level

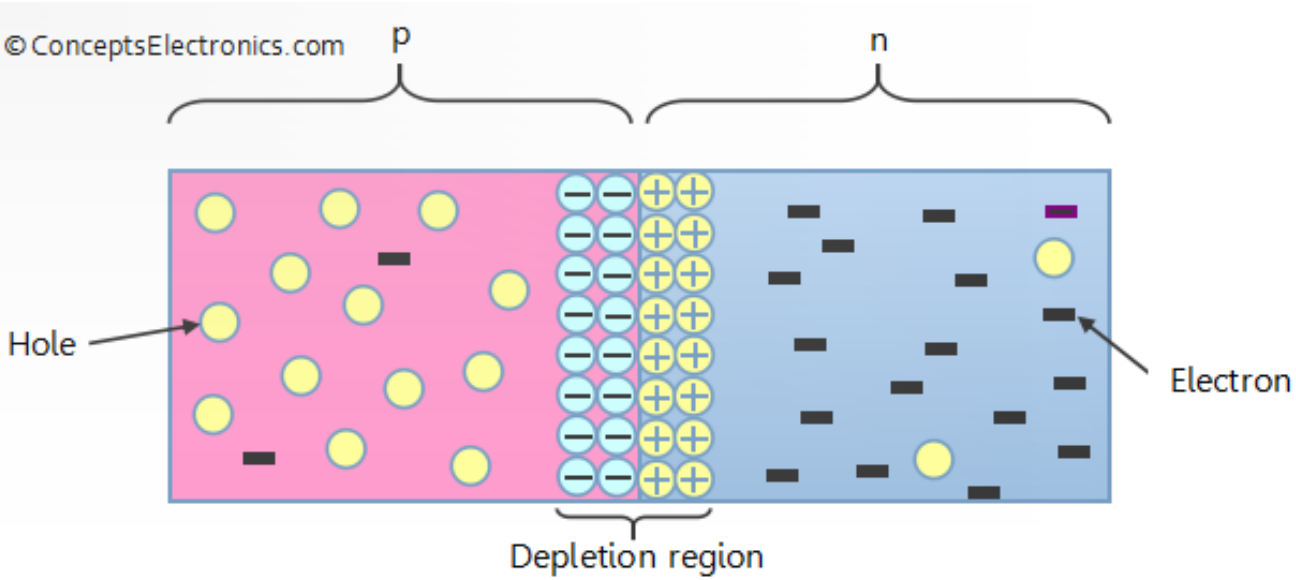
- Circuit Level

Types of Switching Network:

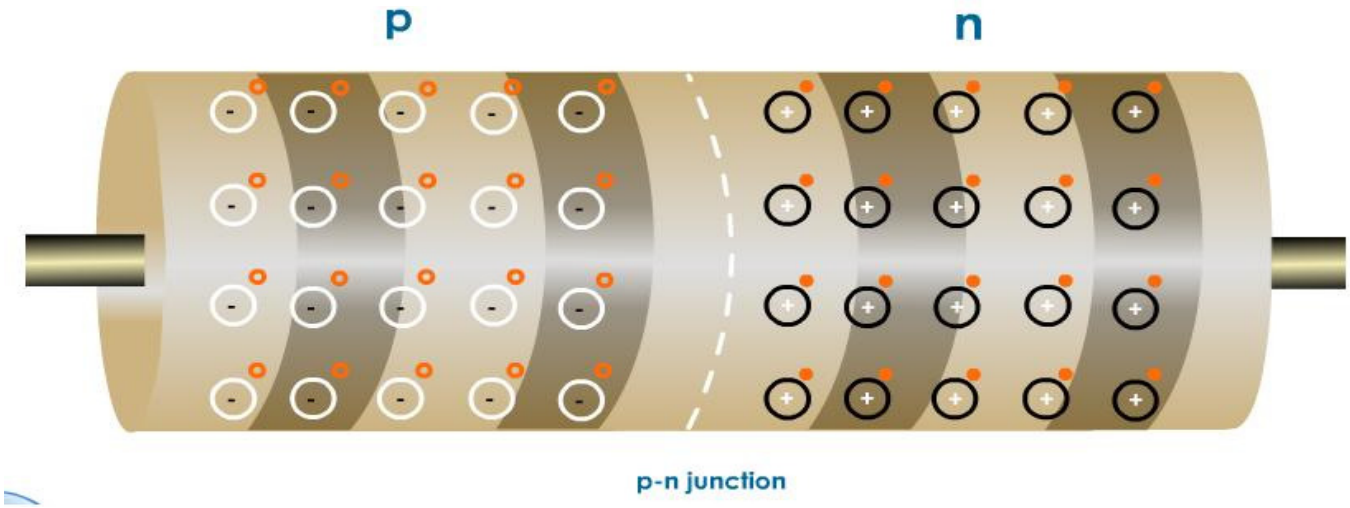
- Combinatorial

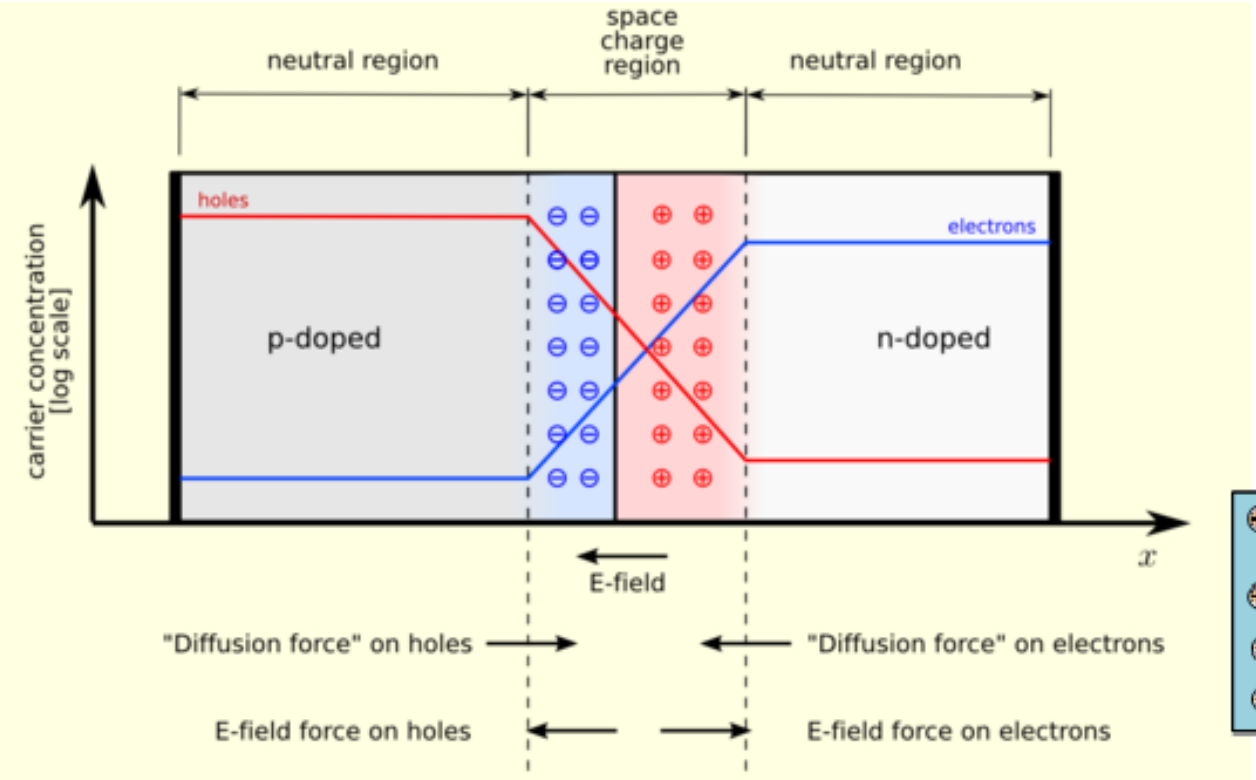
- Sequential

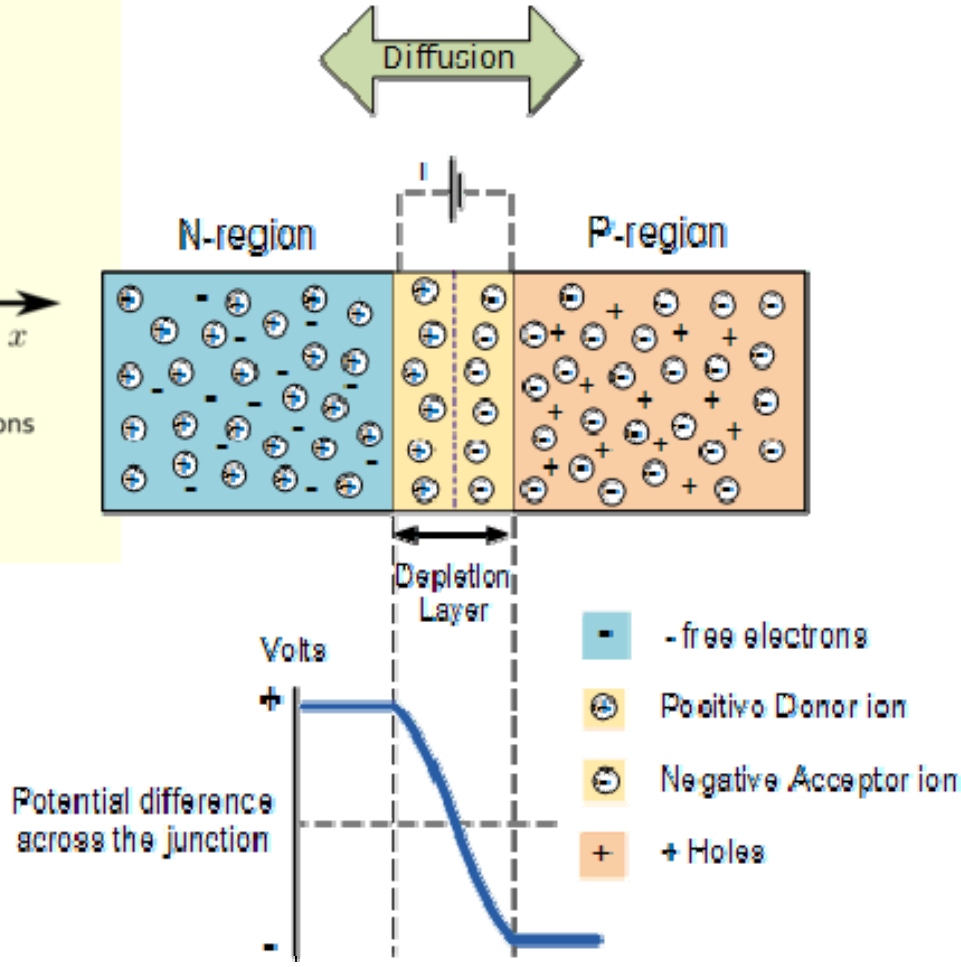
BJT Props. Follow →

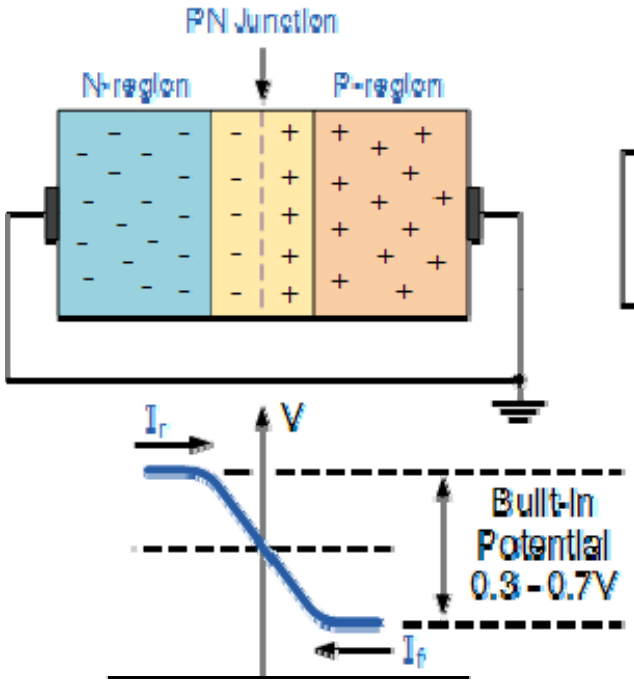


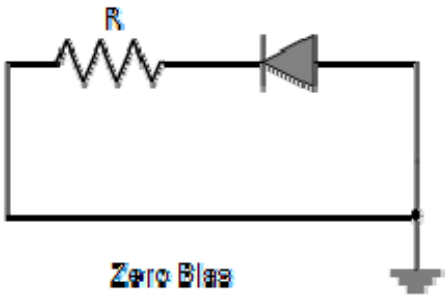
Situation after the formation of depletion region

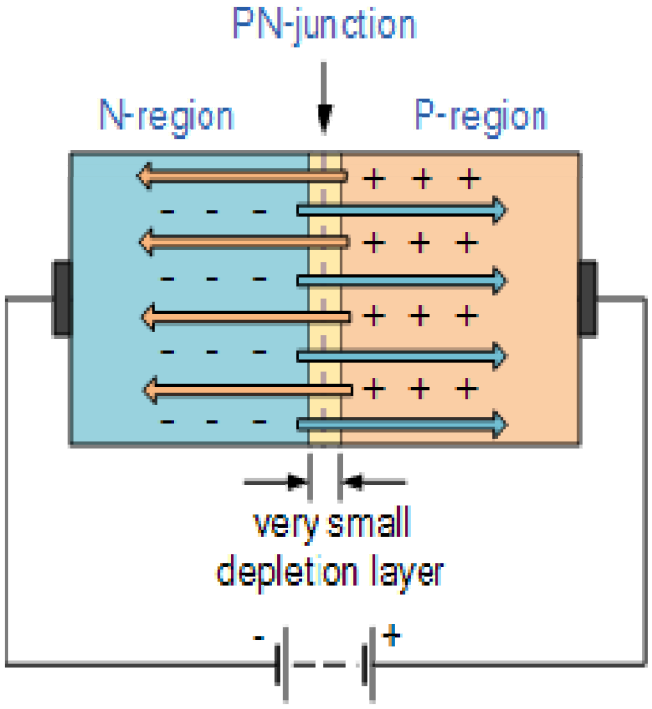



neutral region
space charge region
neutral region
holes
electrons
p-doped
n-doped
carrier concentration [log scale]
x
E-field
"Diffusion force" on holes
"Diffusion force" on electrons
E-field force on holes
E-field force on electrons

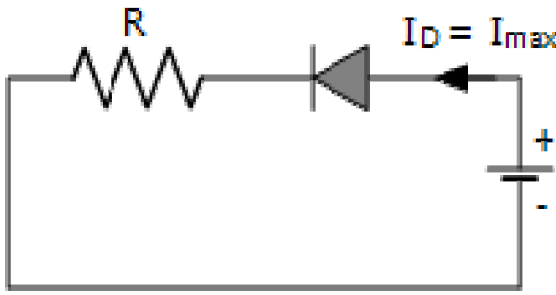

Diffusion
N-region
P-region
Depletion Layer
Volts
+
-
Potential difference across the junction
- free electrons
Positive Donor ion
Negative Acceptor ion
+ Holes

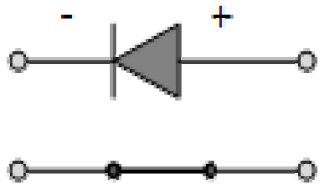


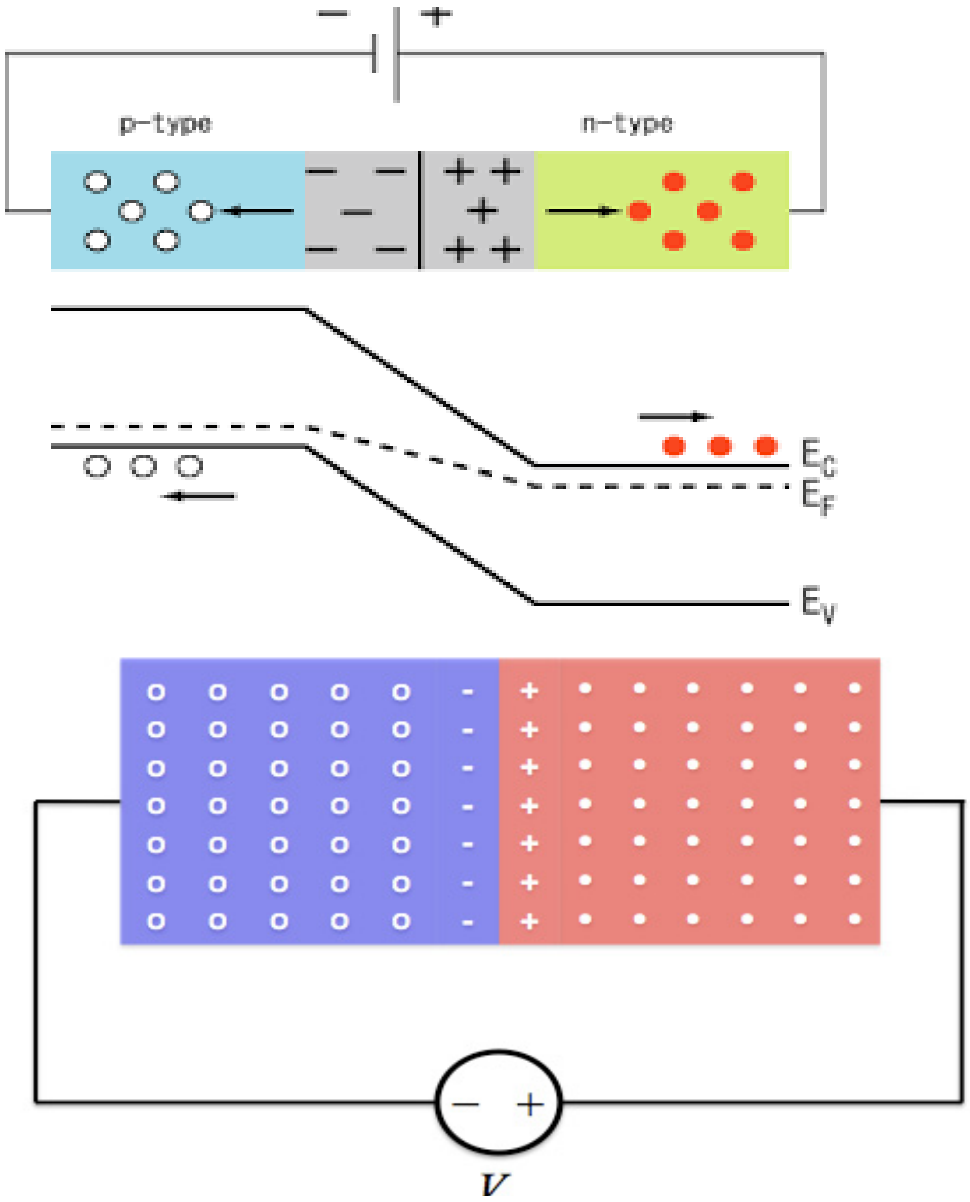


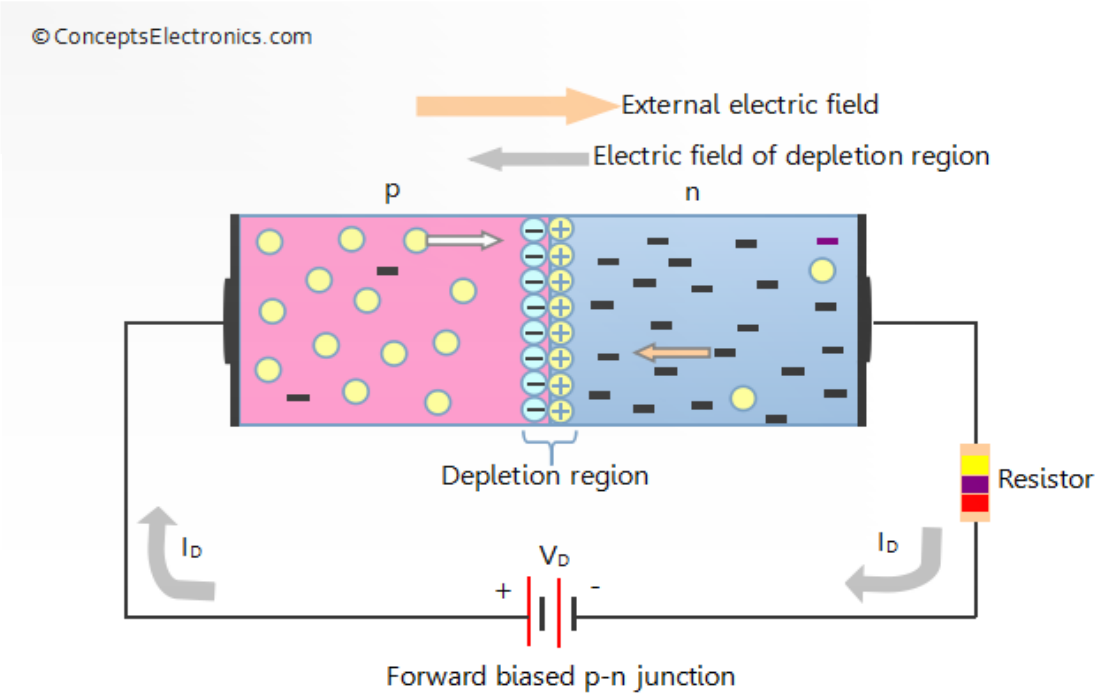


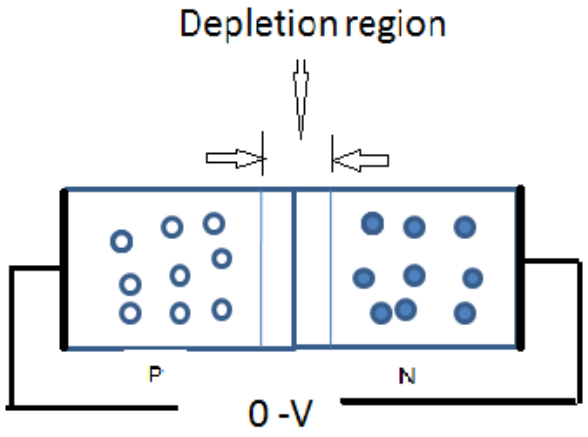
Forward Biasing Voltage



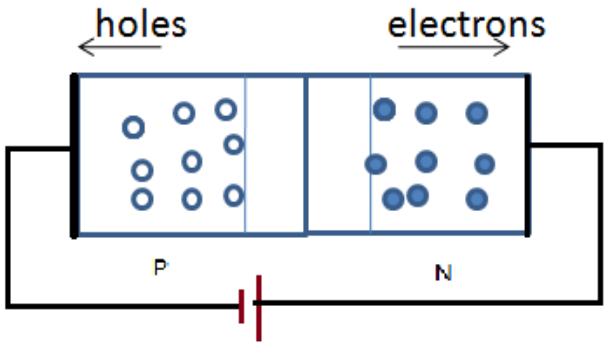



p-type
n-type
E_C
E_F
E_V
V

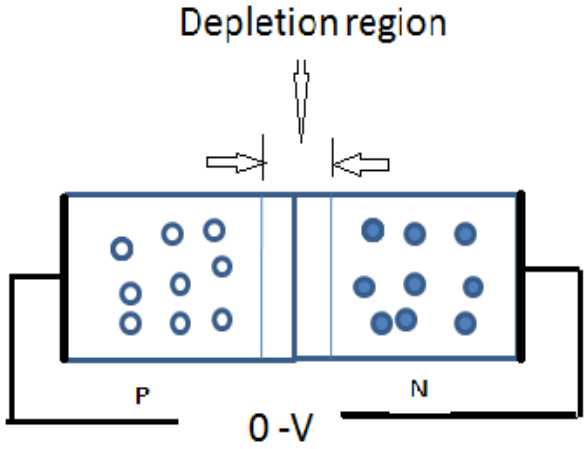

© ConceptsElectronics.com
External electric field
Electric field of depletion region
p
n
Depletion region
Resistor
I_D
V_D
I_D
+
-
Forward biased p-n junction



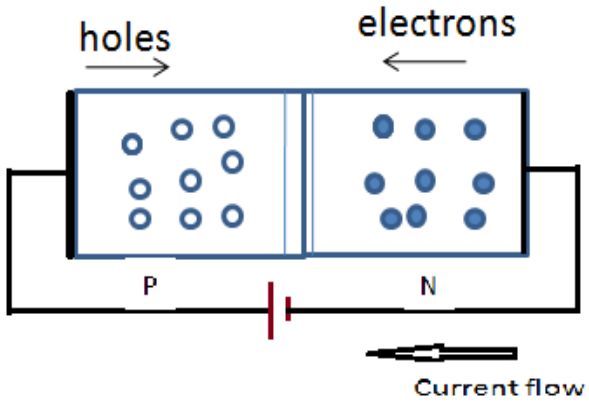
Without bias voltage



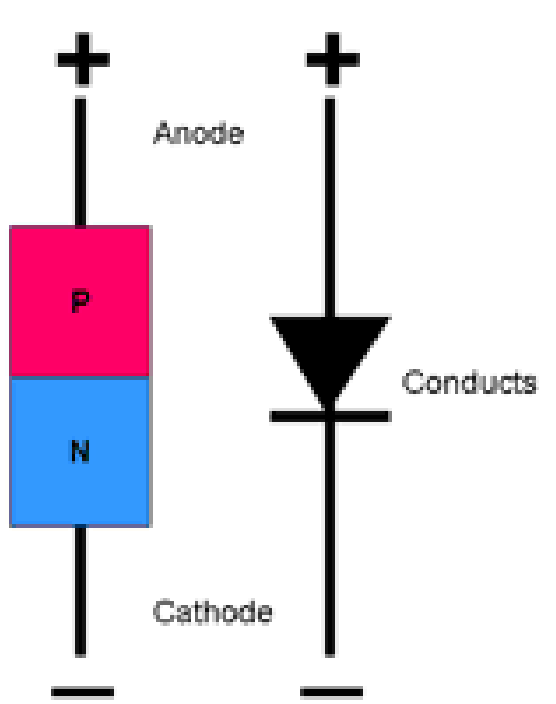
With Reverse bias voltage



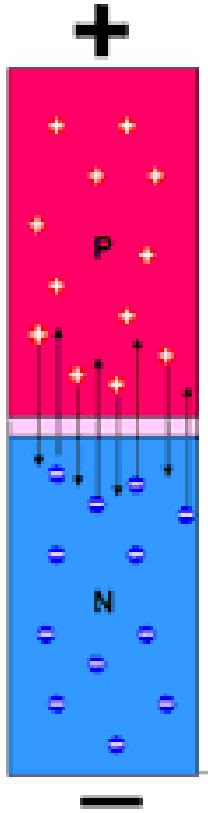
Without bias voltage

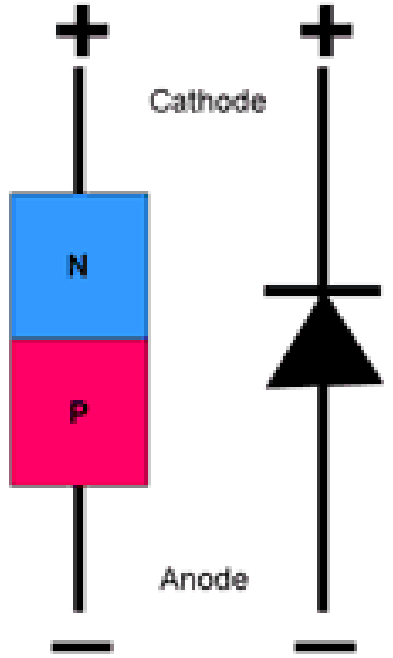


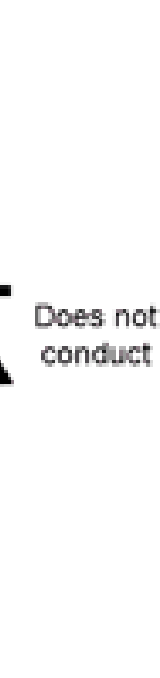
With forward bias voltage

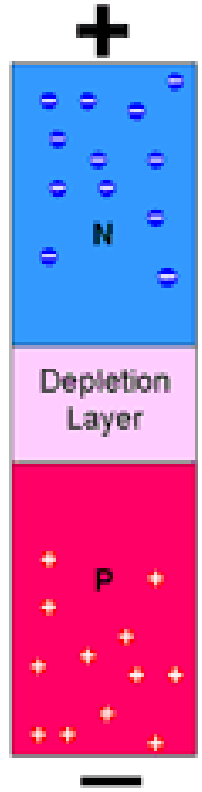


Diode (P-N Junction)
Forward Biased

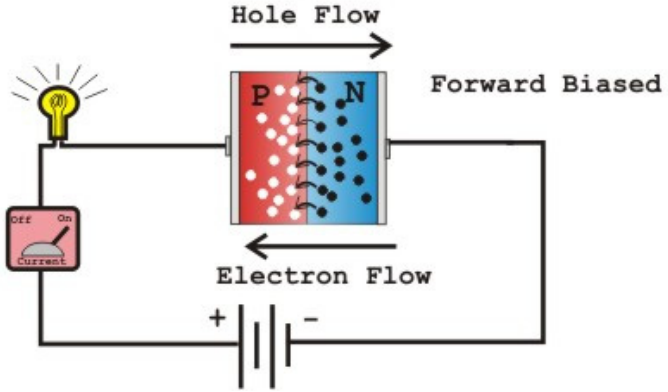


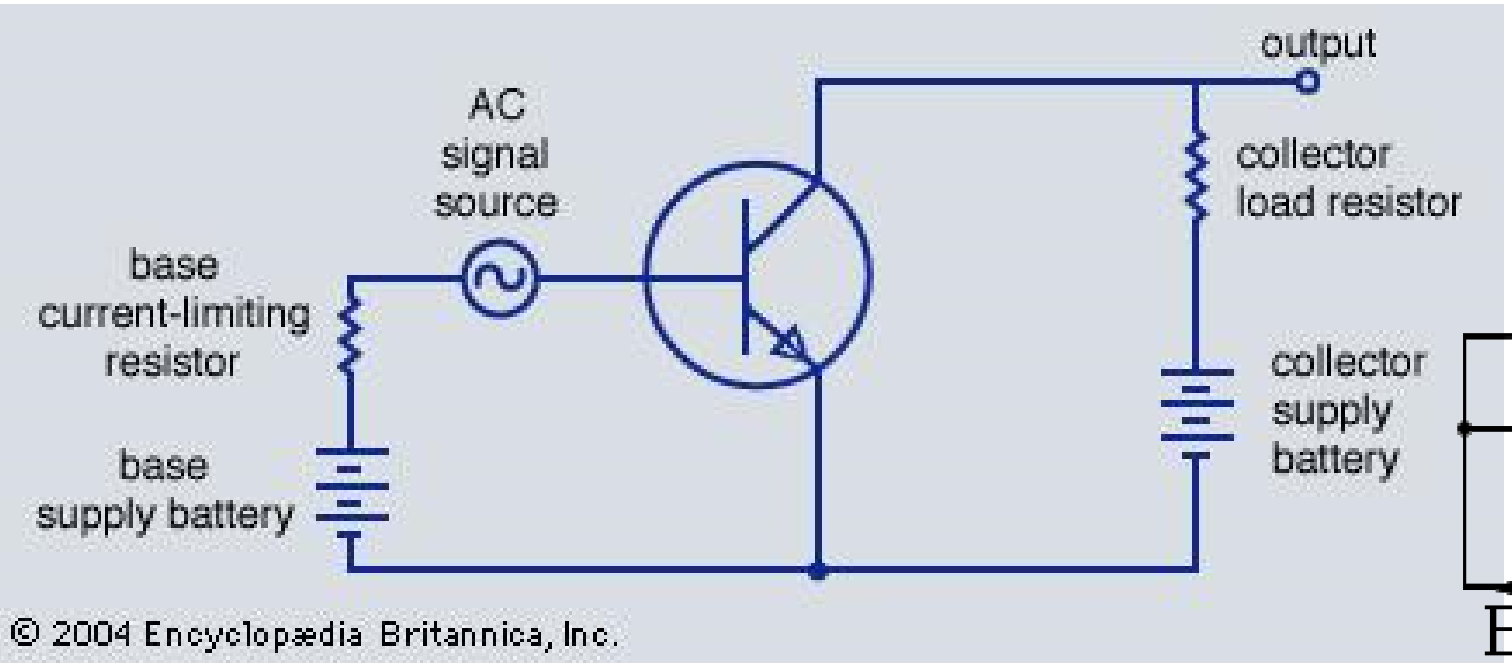


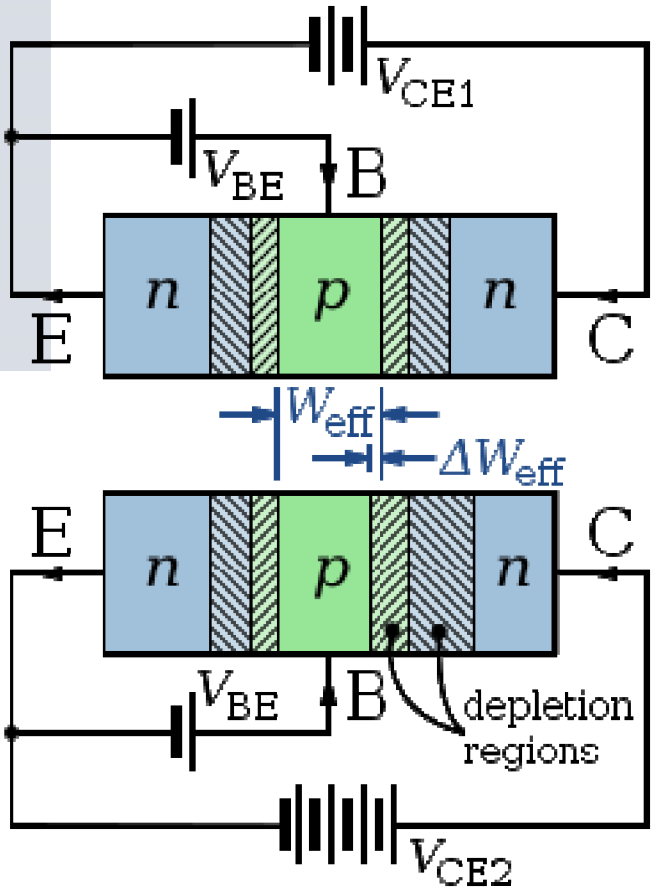


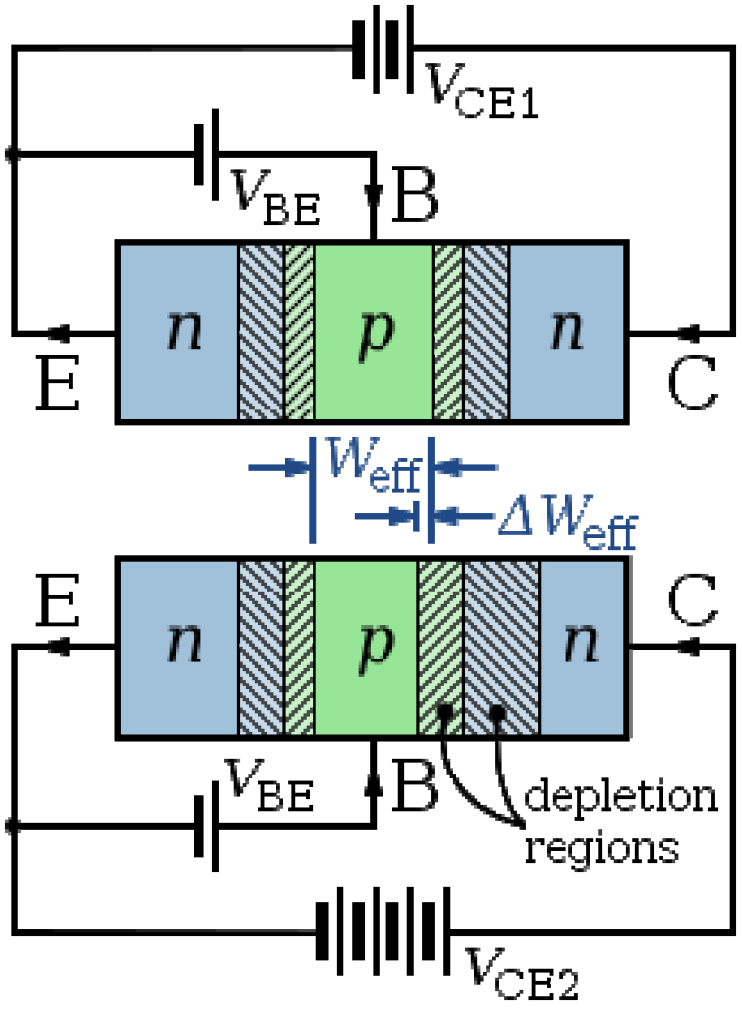


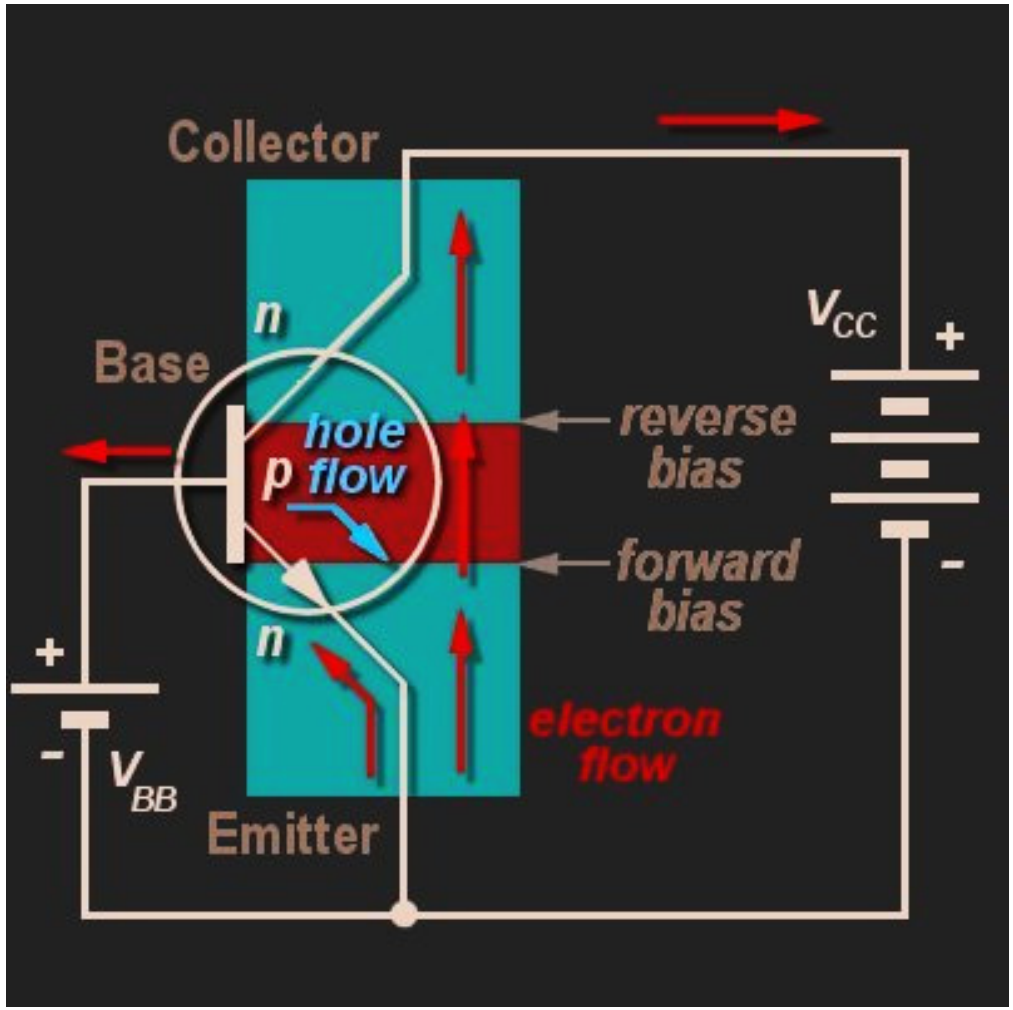
Diode (P-N Junction)
Reverse biased

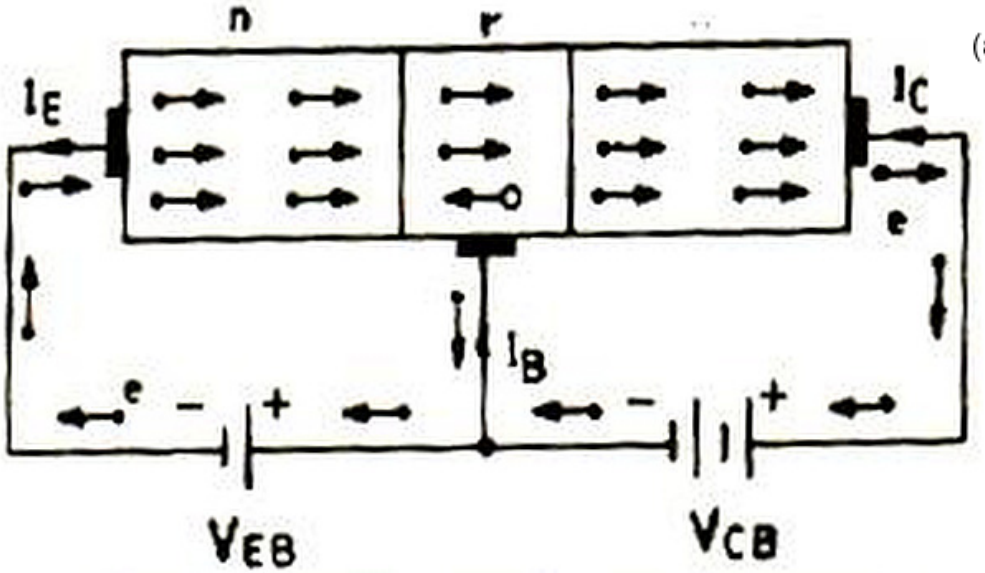



output
AC
signal
source
collector
load resistor
base
current-limiting
resistor
collector
supply
battery
base
supply battery
© 2004 Encyclopædia Britannica, Inc.

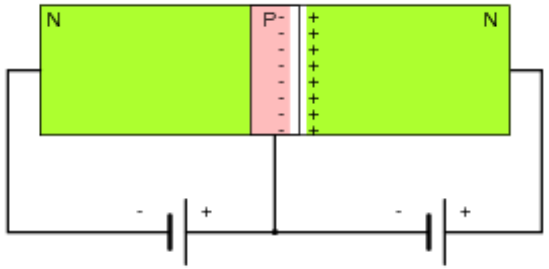

V_{CE1}
V_{BE}
B
n
p
n
E
C
W_{eff}
ΔW_{eff}
E
n
p
n
C
V_{BE}
B
depletion
regions
V_{CE2}


V_{CE1}
V_{BE}
B
n
p
n
E
C
W_{eff}
ΔW_{eff}
E
n
p
n
C
V_{BE}
B
depletion regions
V_{CE2}

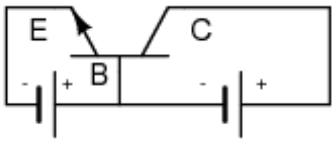

Collector
n
Base
hole
p flow
reverse
bias
forward
bias
n
V_{CC}
+
-
+
-
V_{BB}
electron
flow
Emitter

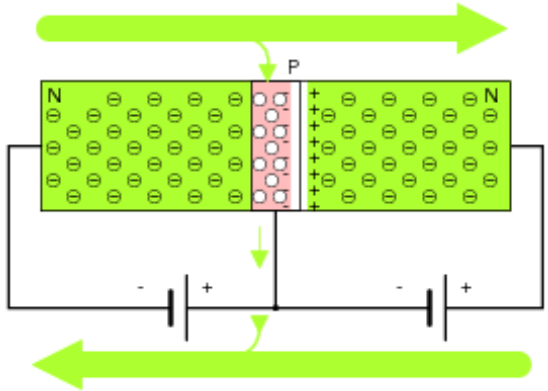


Basic Connections of n-p-n Transistor

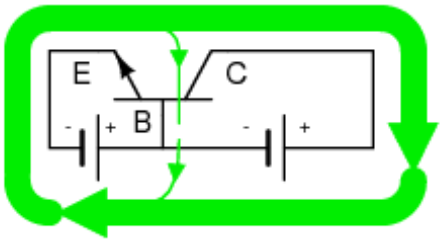


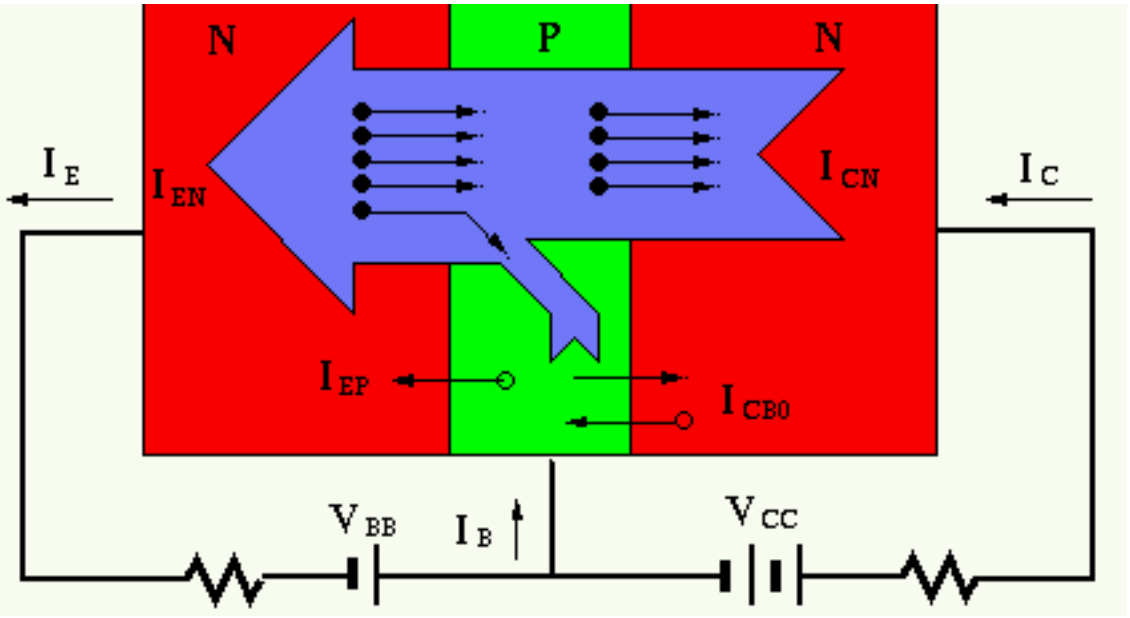
(a)

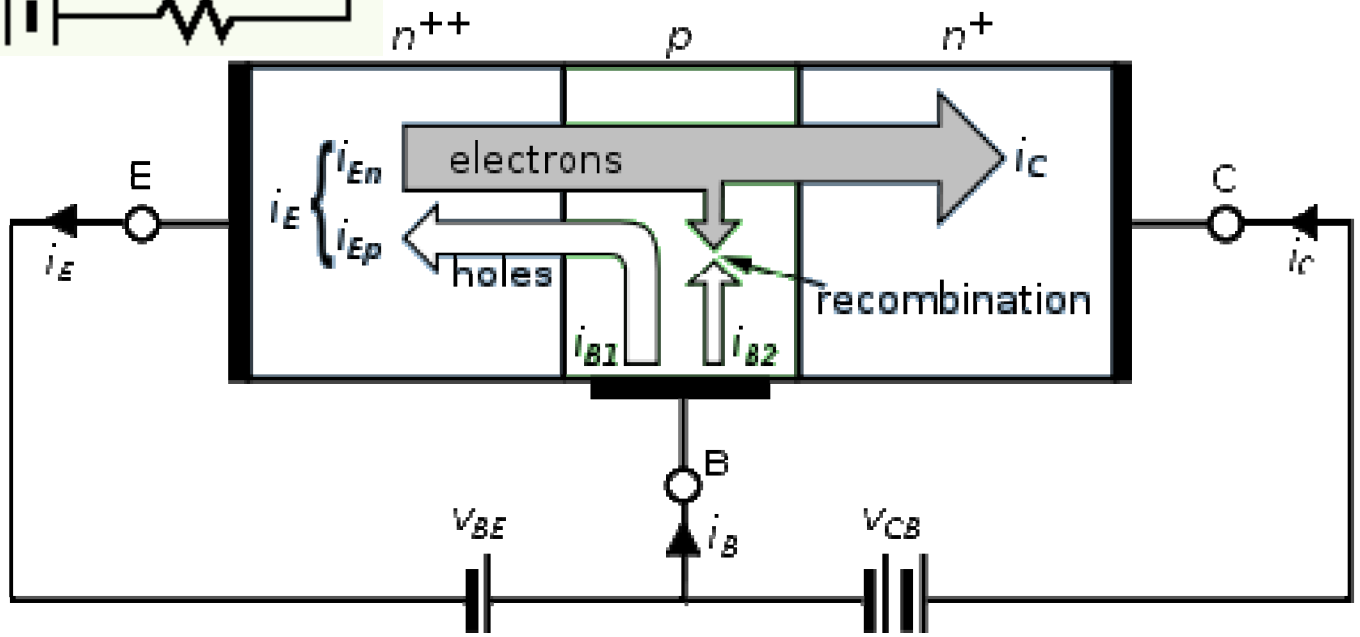


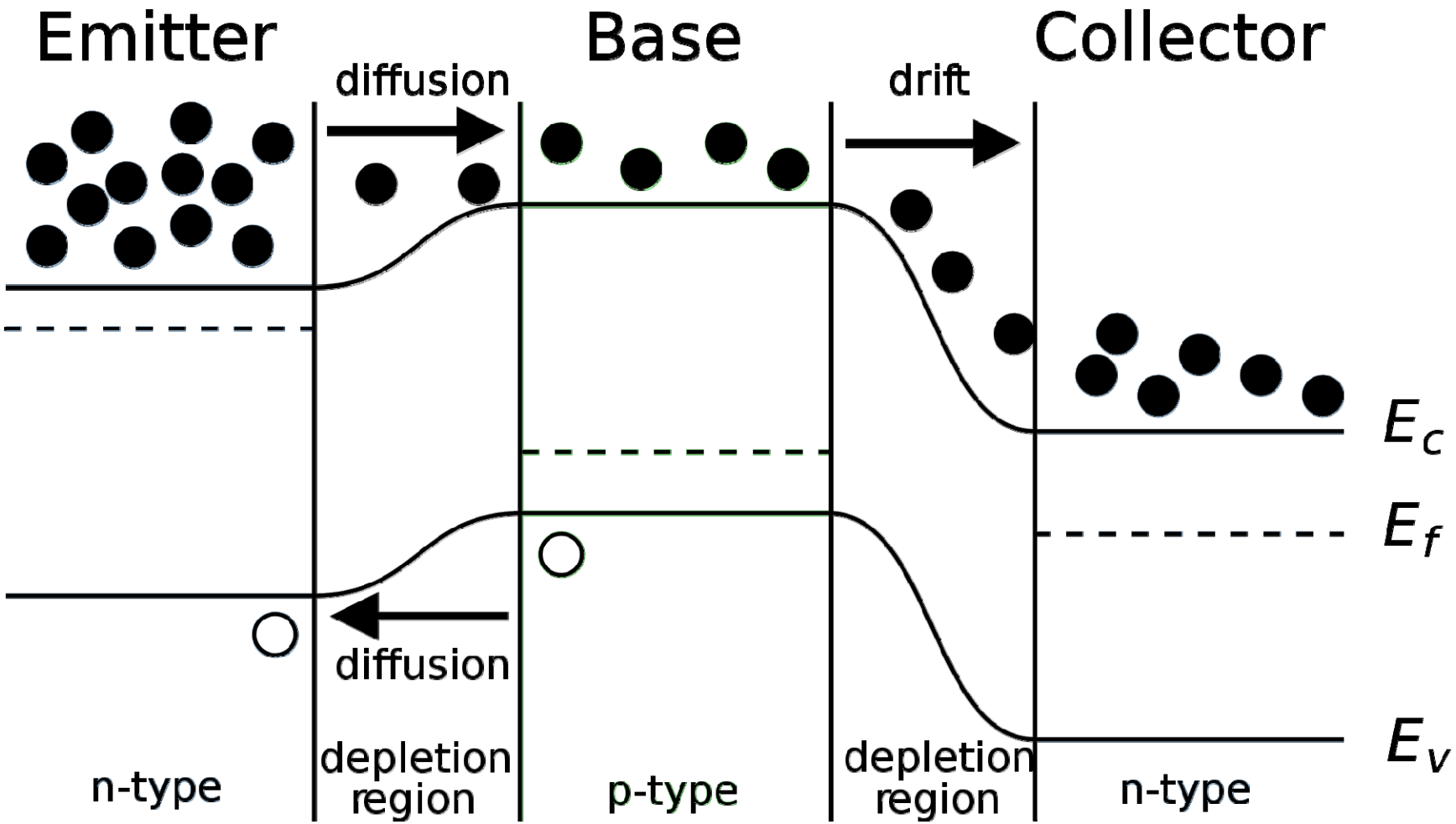


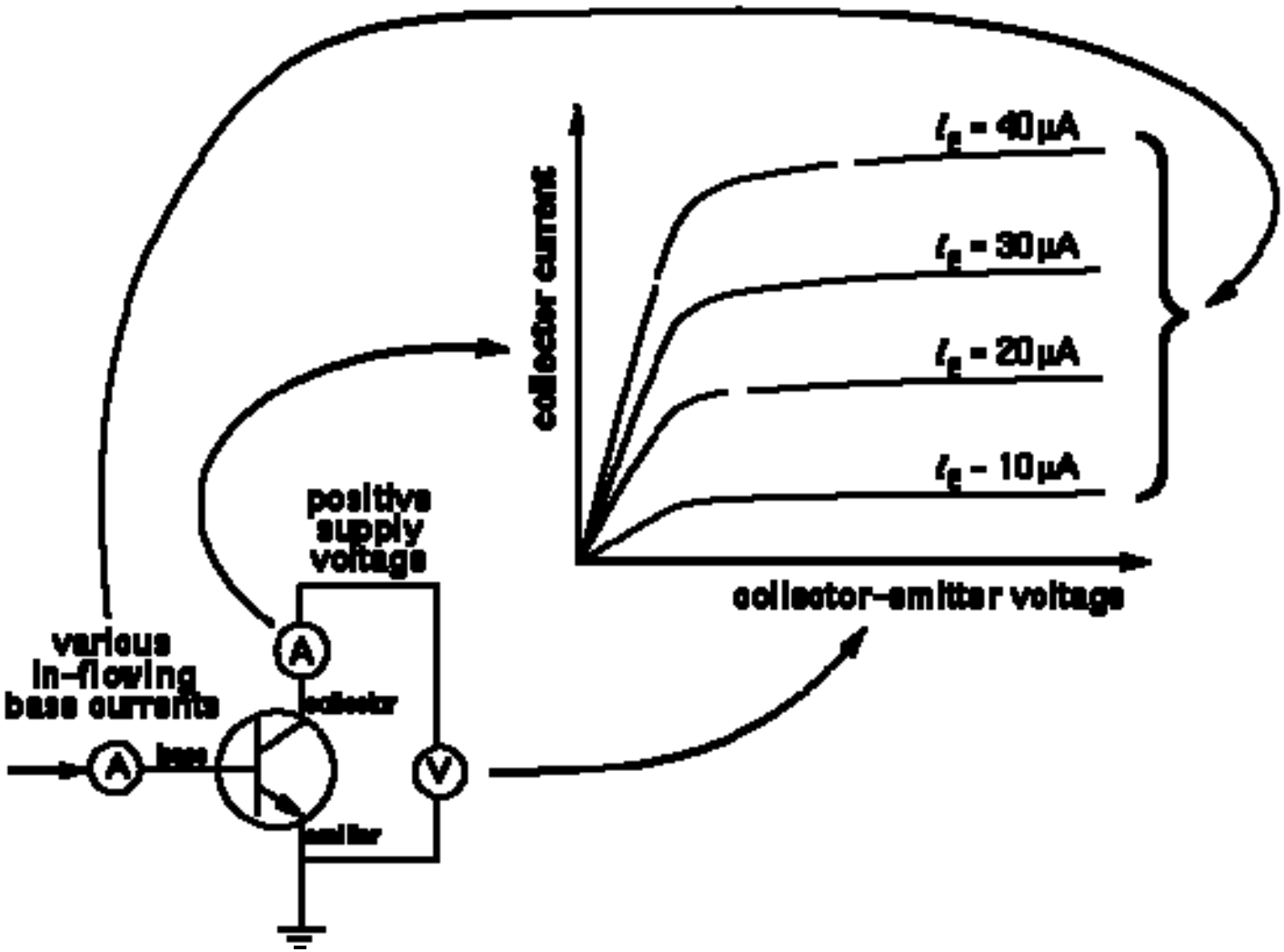
(b)



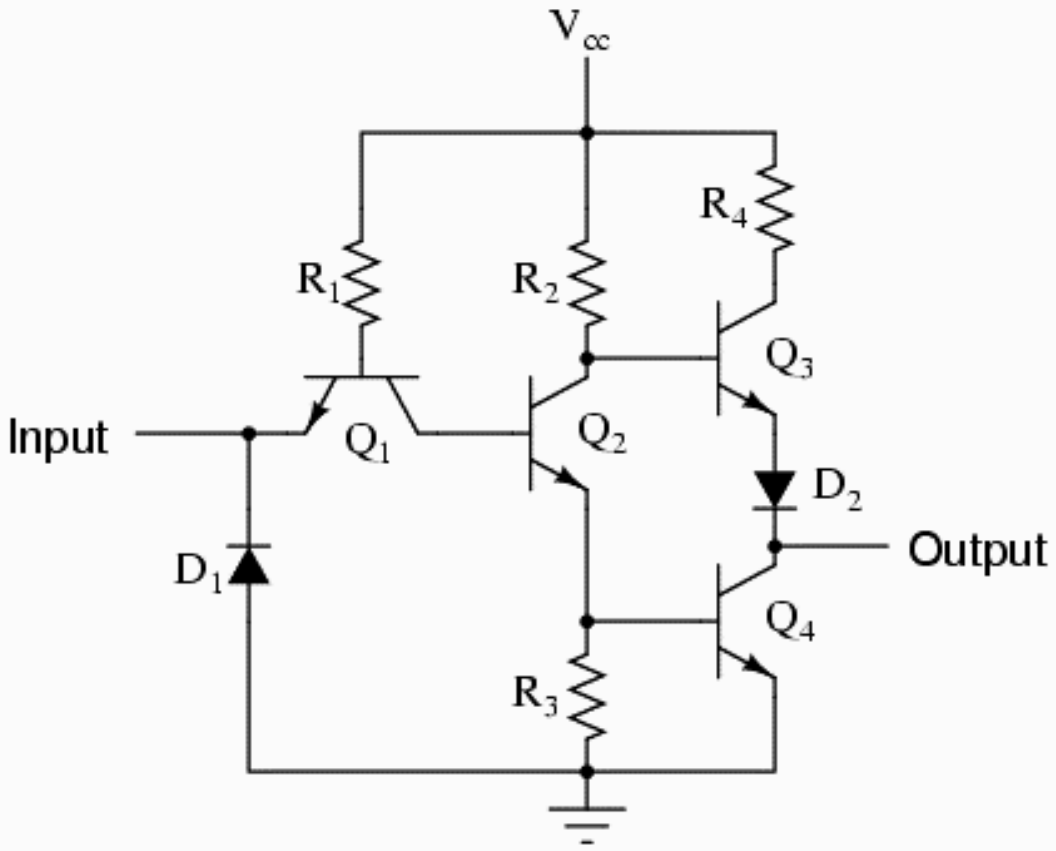

N
P
N
I E
I EN
I CN
I C
I EP
I CB0
V BB
I B
V CC

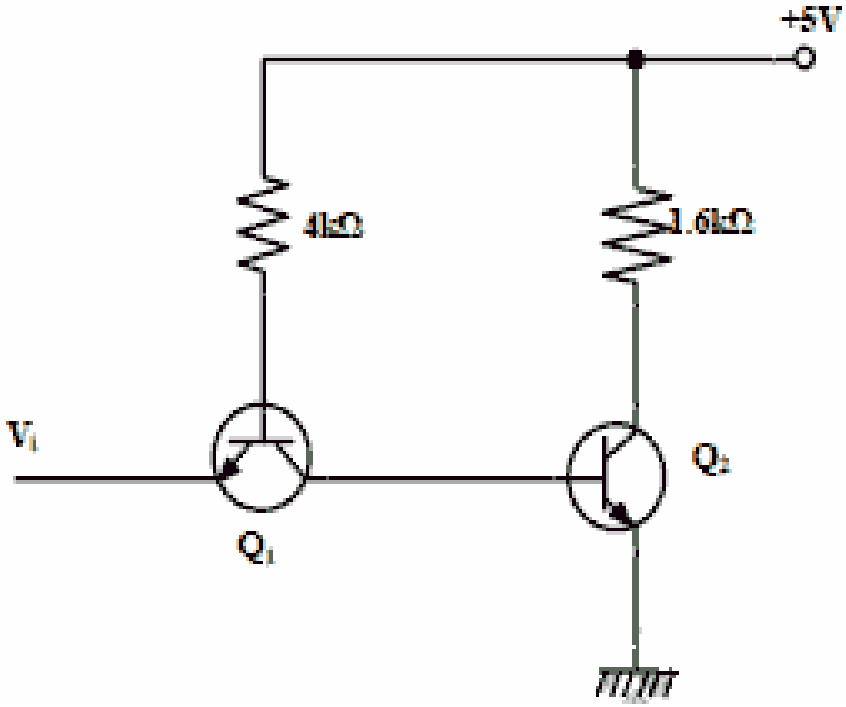

n++
p
n+
E
C
B
electrons
holes
recombination
i_E
i_{En}
i_{Ep}
i_C
i_{B1}
i_{B2}
i_B
V_{BE}
V_{CB}

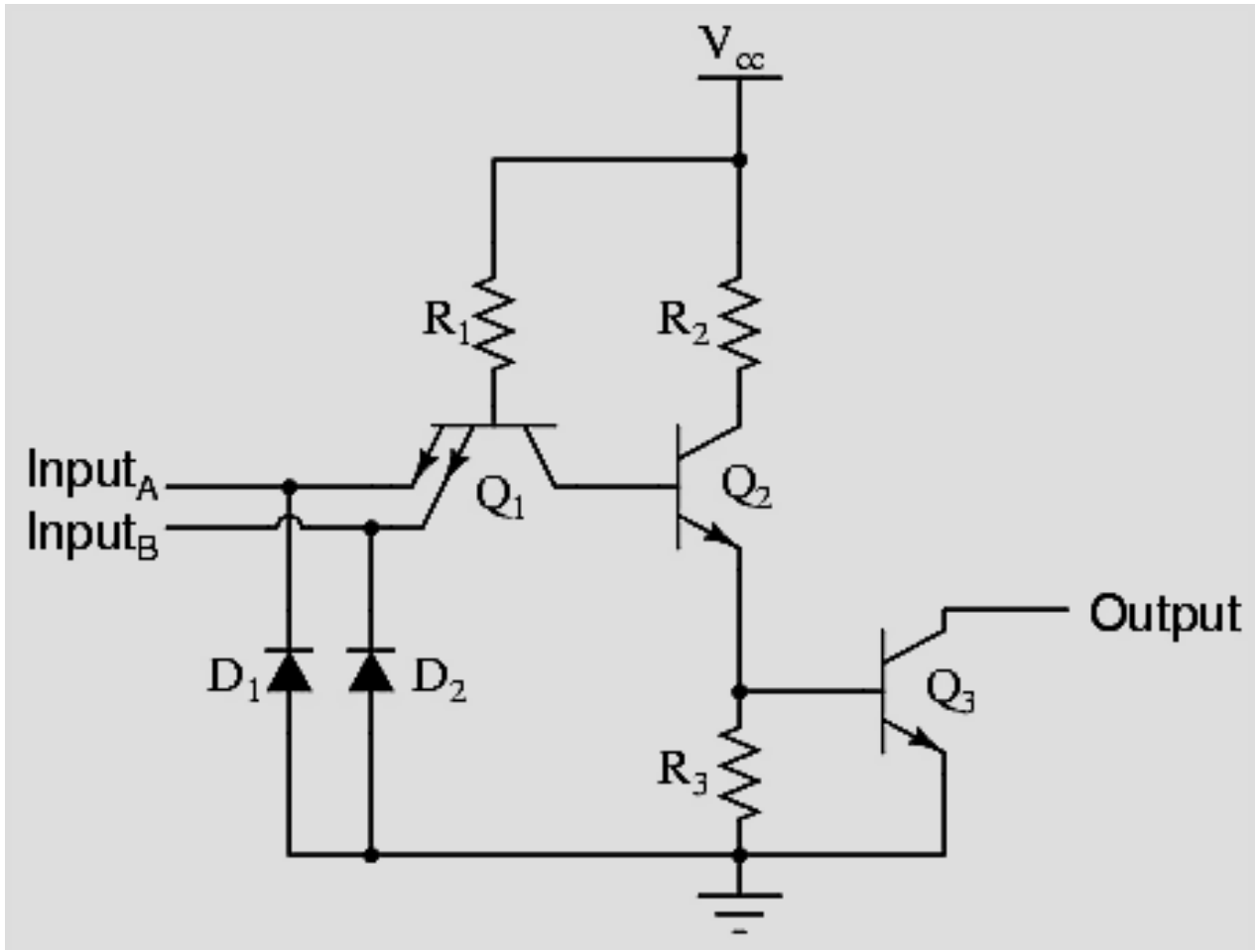

Emitter
Base
Collector
diffusion
drift
diffusion
E_c
E_f
E_v
n-type
depletion region
p-type
depletion region
n-type


I_B = 40 µA
I_B = 30 µA
I_B = 20 µA
I_B = 10 µA
collector current
collector-emitter voltage
positive supply voltage
various in-flowing base currents
A
V
collector
base
emitter

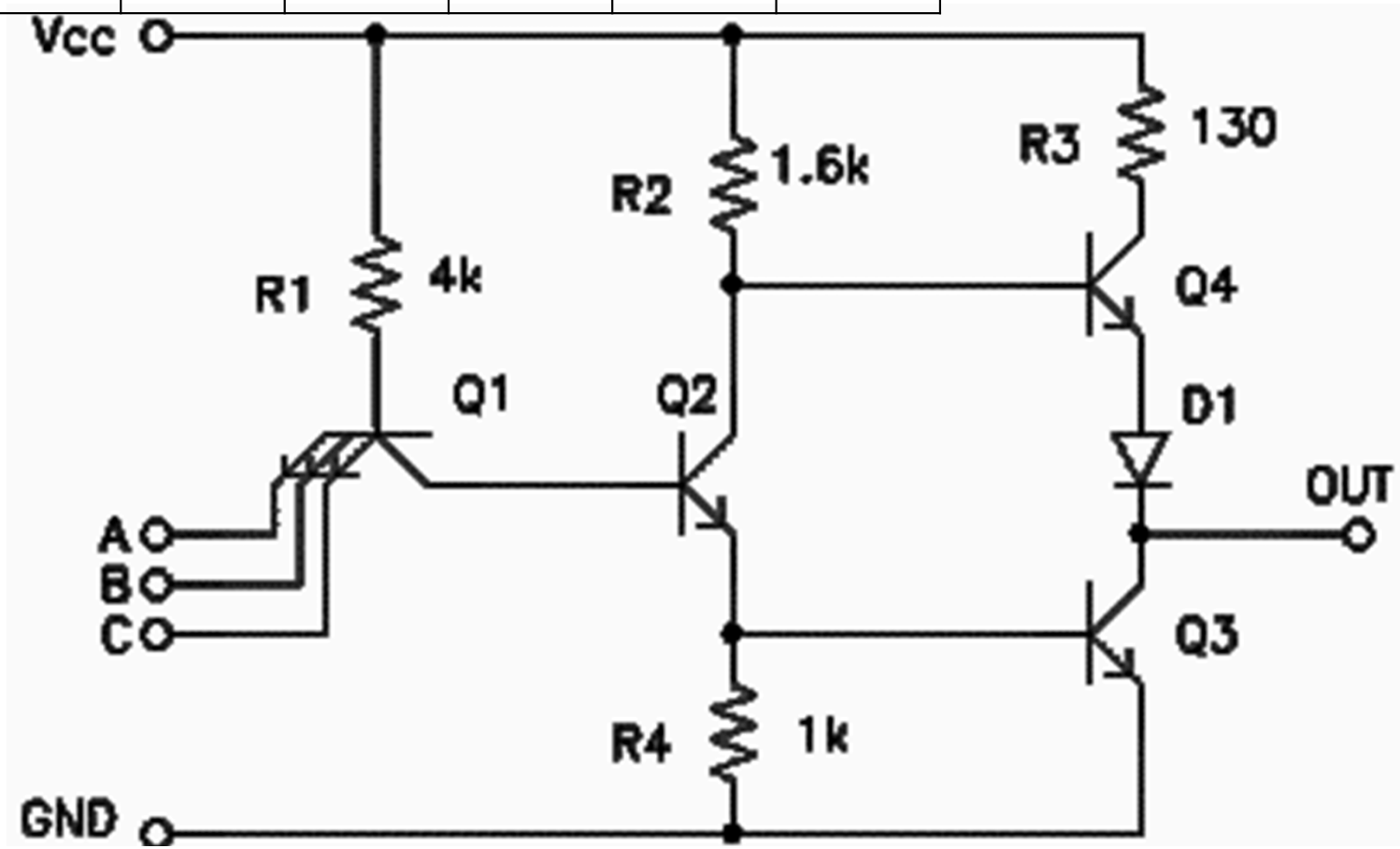
Practical inverter (NOT) circuit

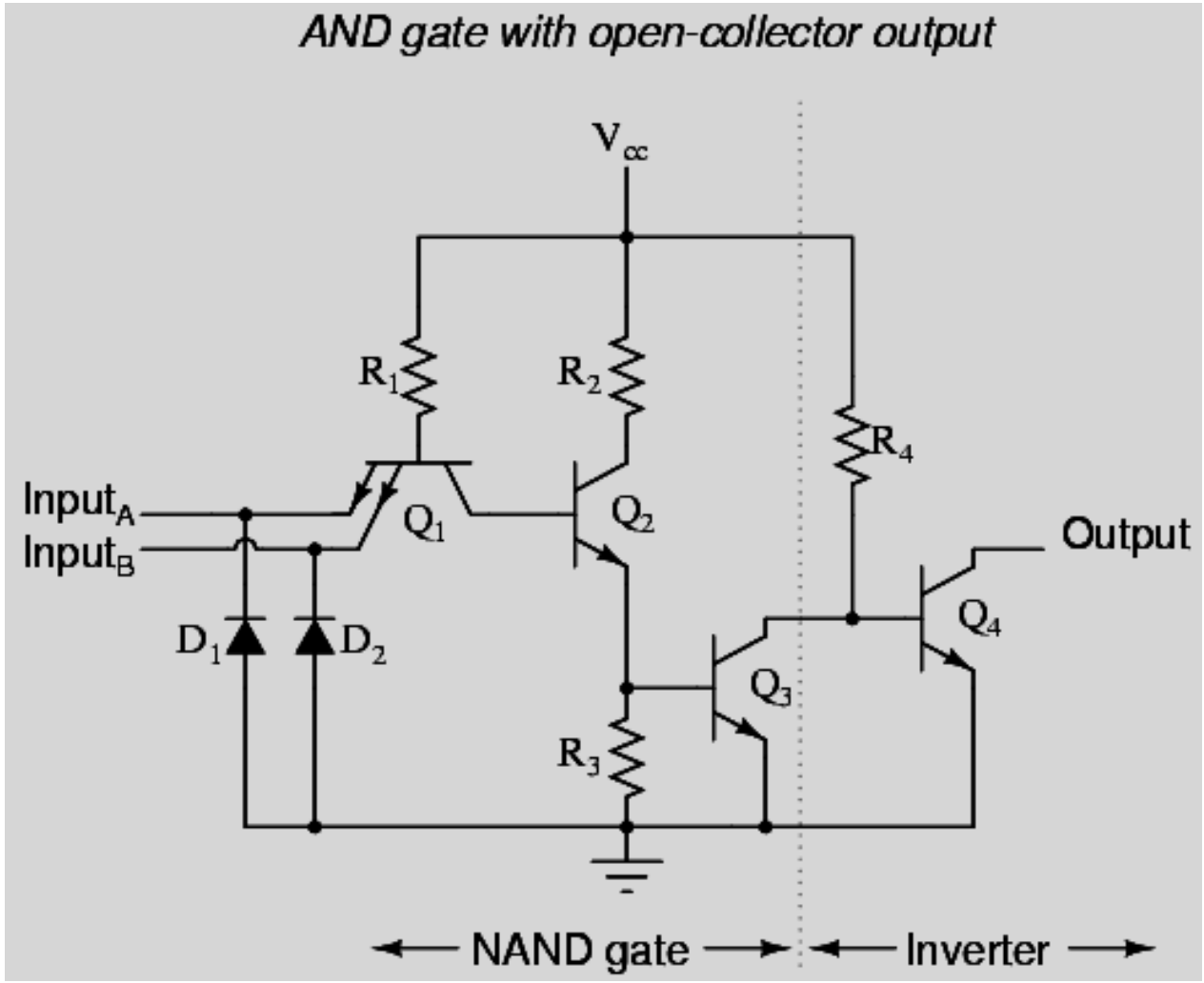


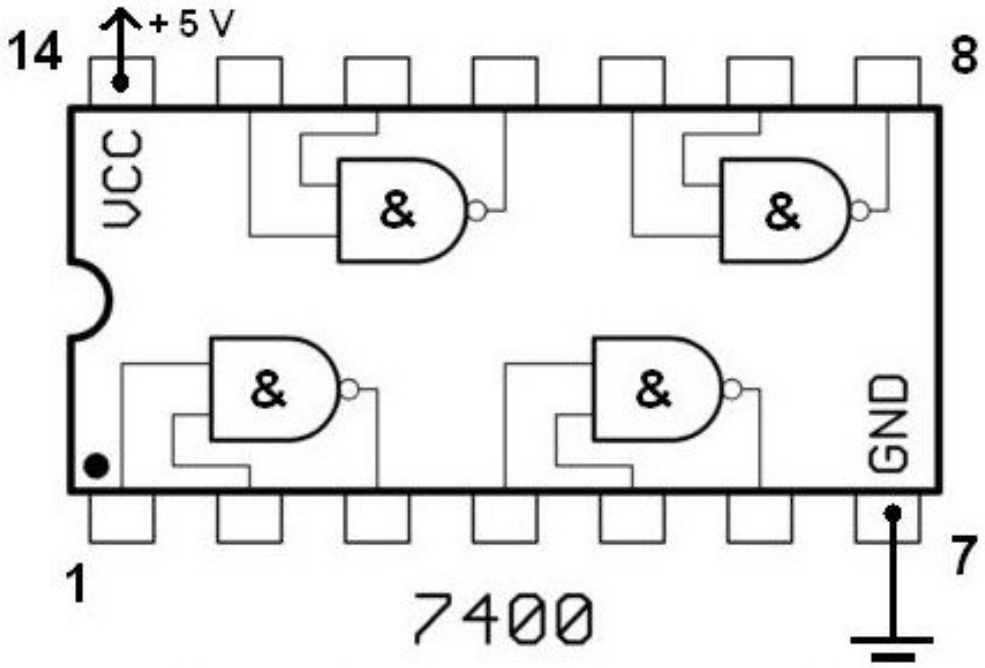


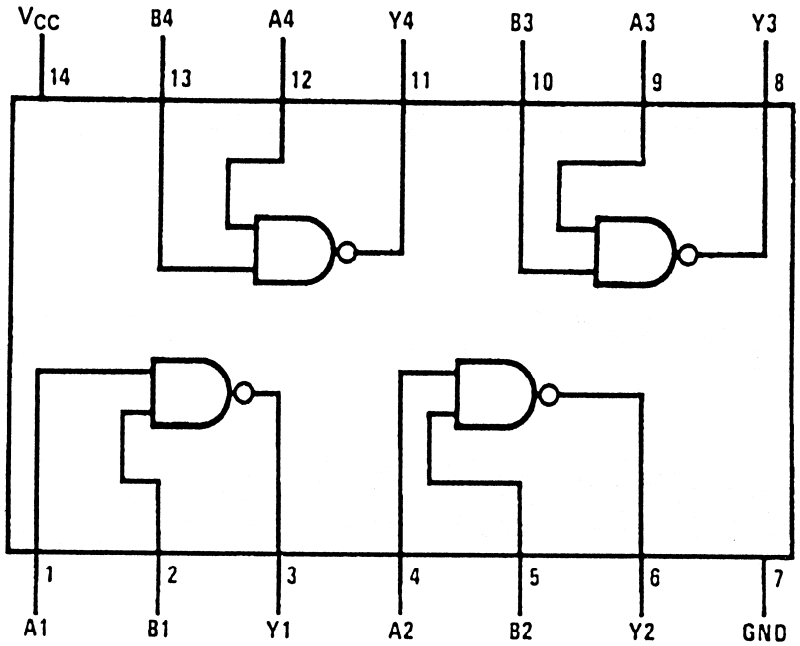

V_{cc}
R_1
R_2
$Input_A$
$Input_B$
Q_1
Q_2
Output
D_1
D_2
Q_3
R_3

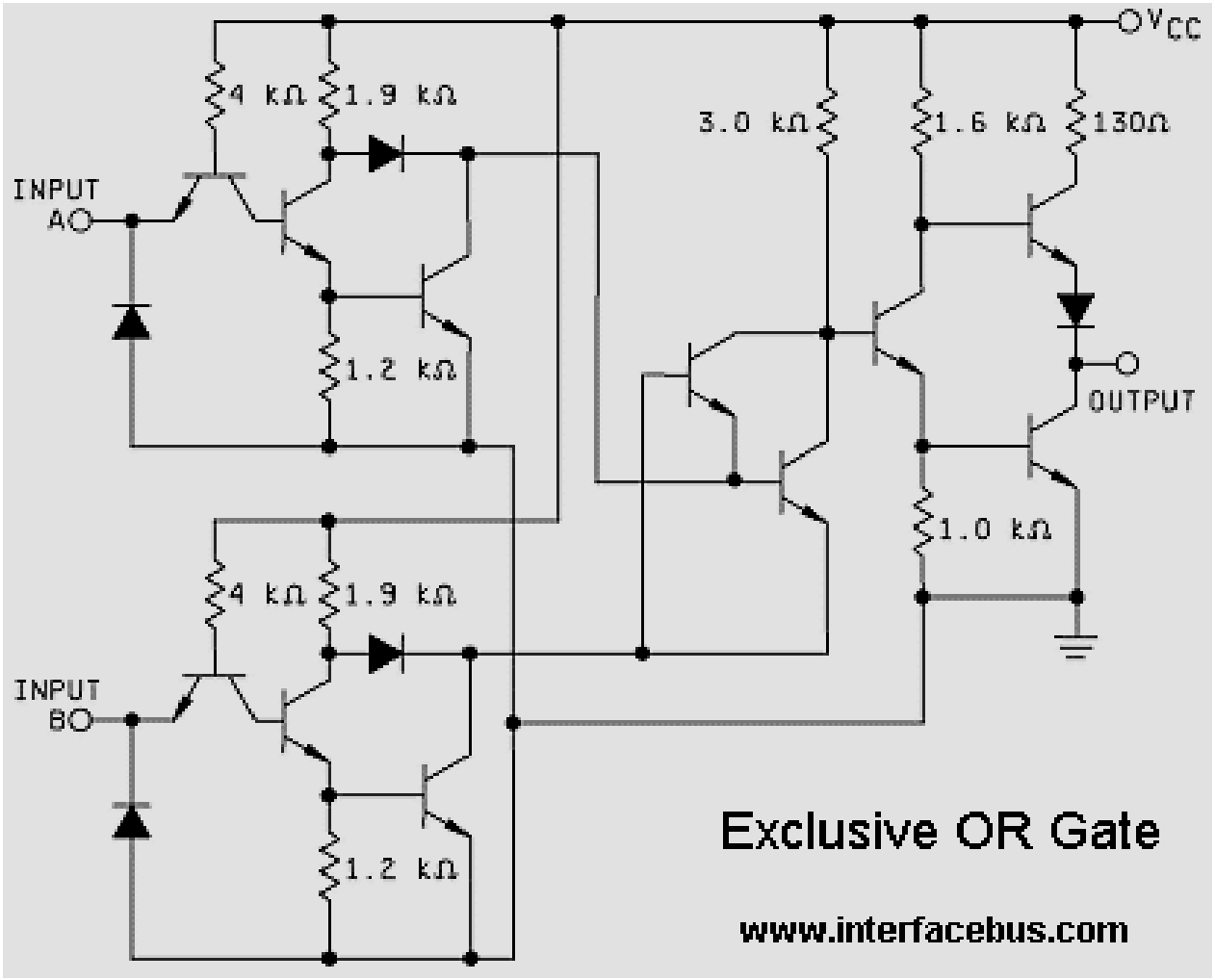
	A, B, C	Q 1	Q 2	Q 3	Q 4	D1	OUT	
	1, 1, 1	Diode, B->C	SATN	SATN	OFF	OFF	LOW	
	Any or all "0"	ON	OFF	OFF	ON	ON	HIGH	



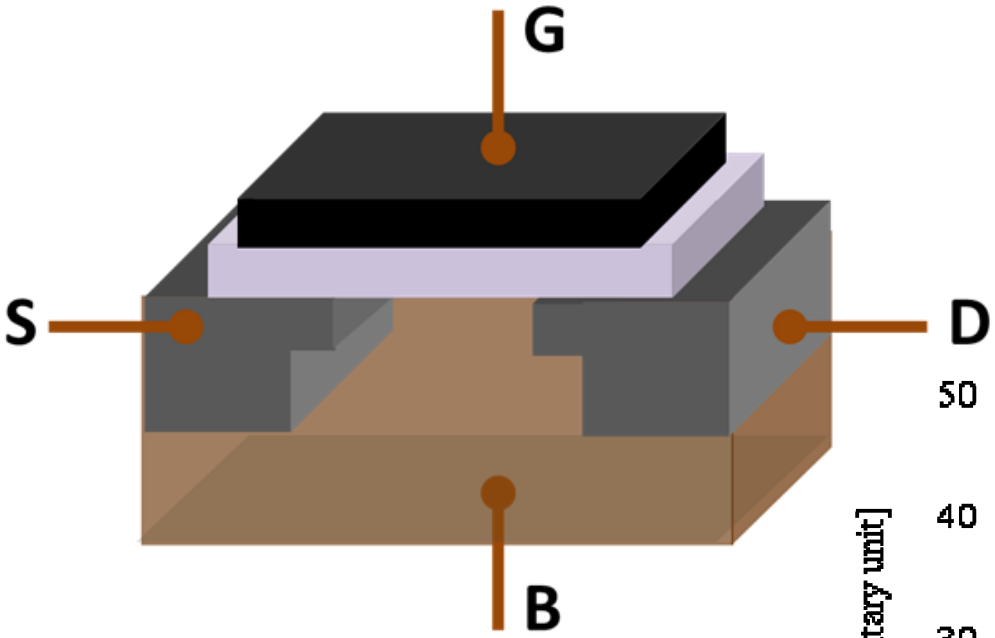

AND gate with open-collector output
Vcc
R1
R2
R4
Input A
Input B
Q1
Q2
Output
D1
D2
Q4
Q3
R3
NAND gate
Inverter

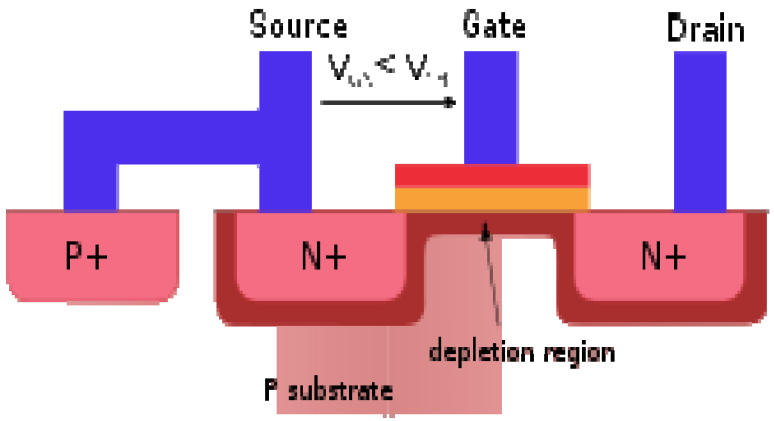

14
+5 V
8
VCC
&
&
&
&
GND
1
7
7400

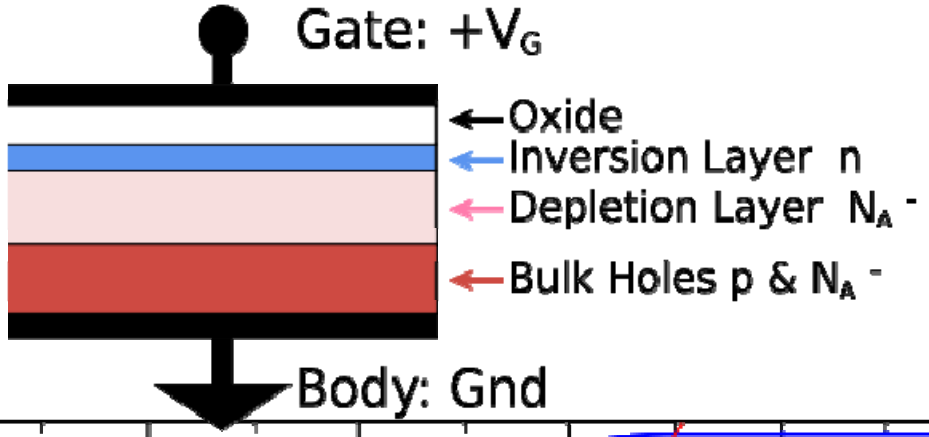

Vcc
B4
A4
Y4
B3
A3
Y3
14
13
12
11
10
9
8
1
2
3
4
5
6
7
A1
B1
Y1
A2
B2
Y2
GND

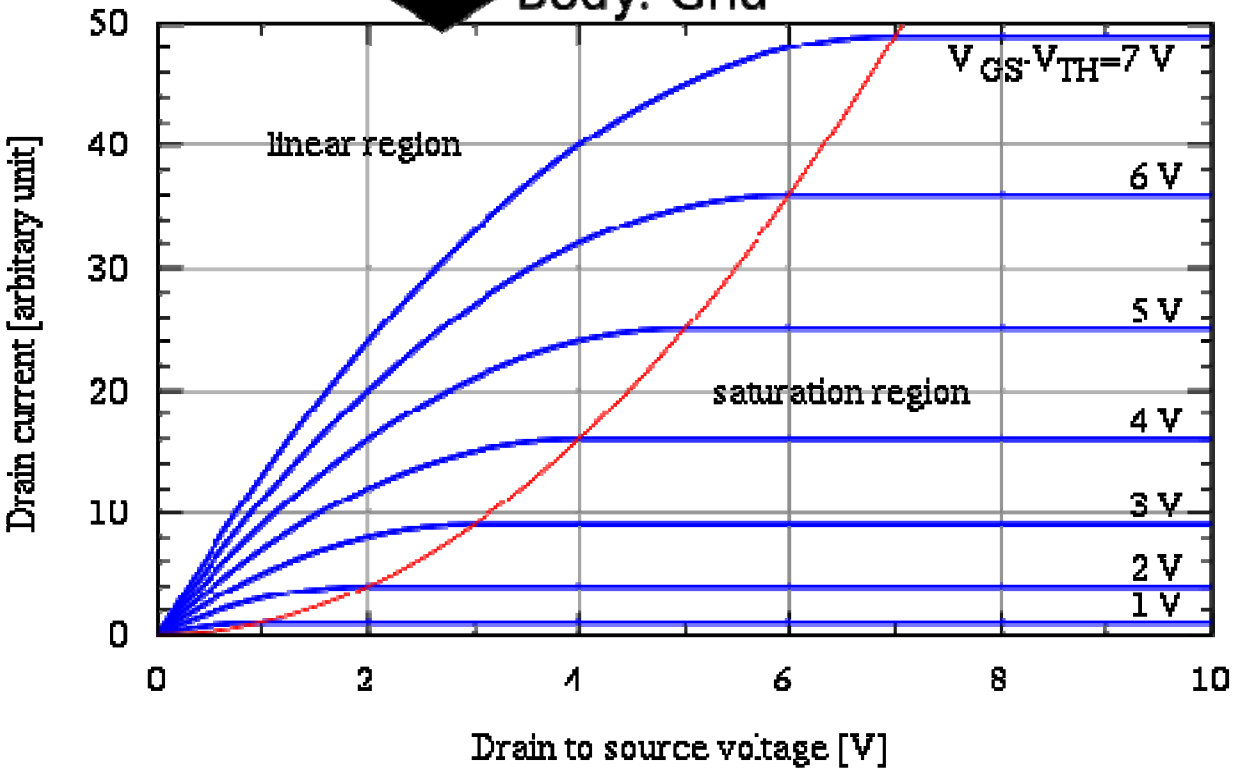

Vcc
4 kΩ
1.9 kΩ
3.0 kΩ
1.6 kΩ
130Ω
INPUT
A
1.2 kΩ
OUTPUT
1.0 kΩ
4 kΩ
1.9 kΩ
INPUT
B
1.2 kΩ
Exclusive OR Gate
www.interfacebus.com

FET → MOSFET → CMOS


G
S
D
B


Source
Gate
Drain
P+
N+
N+
depletion region
P substrate


Gate: +V_G
Oxide
Inversion Layer n
Depletion Layer N_A -
Bulk Holes p & N_A -
Body: Gnd


Drain current [arbitary unit]
Drain to source voltage [V]
linear region
saturation region
V_GS-V_TH=7 V
6 V
5 V
4 V
3 V
2 V
1 V
0
10
20
30
40
50
0
2
4
6
8
10

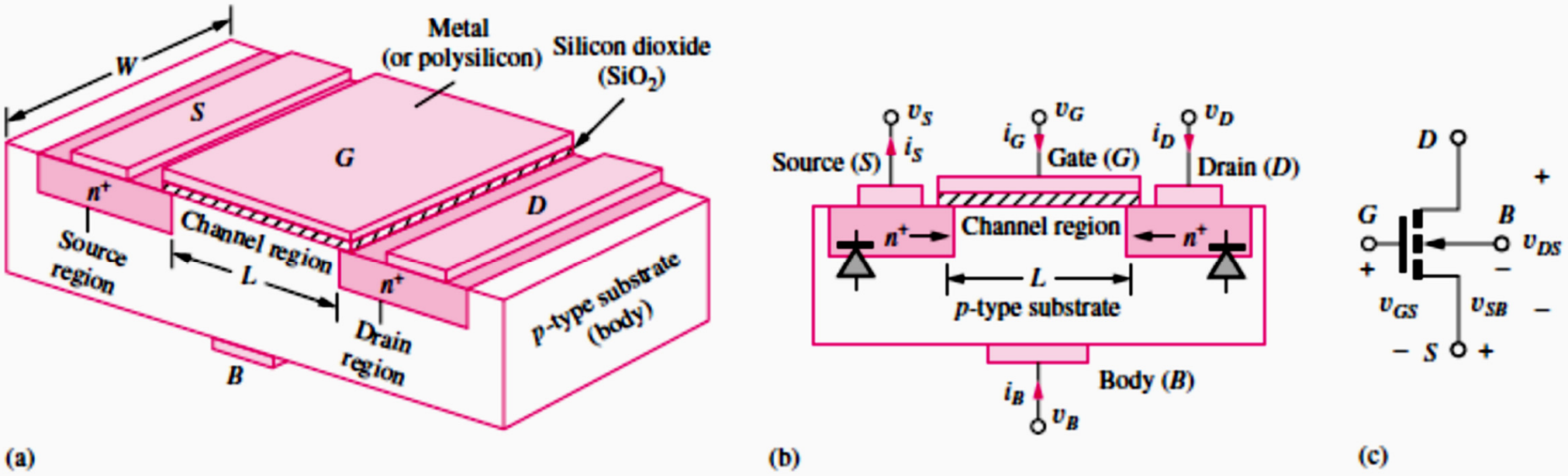
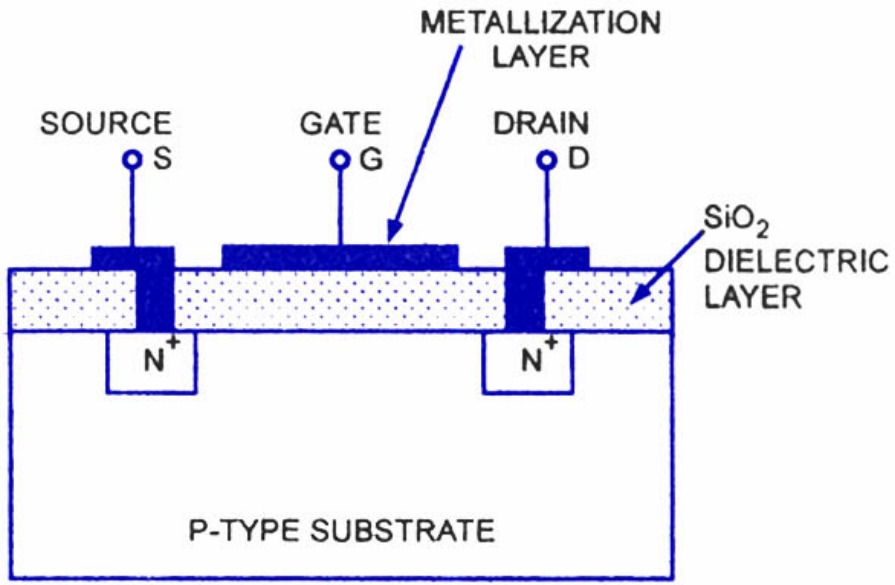
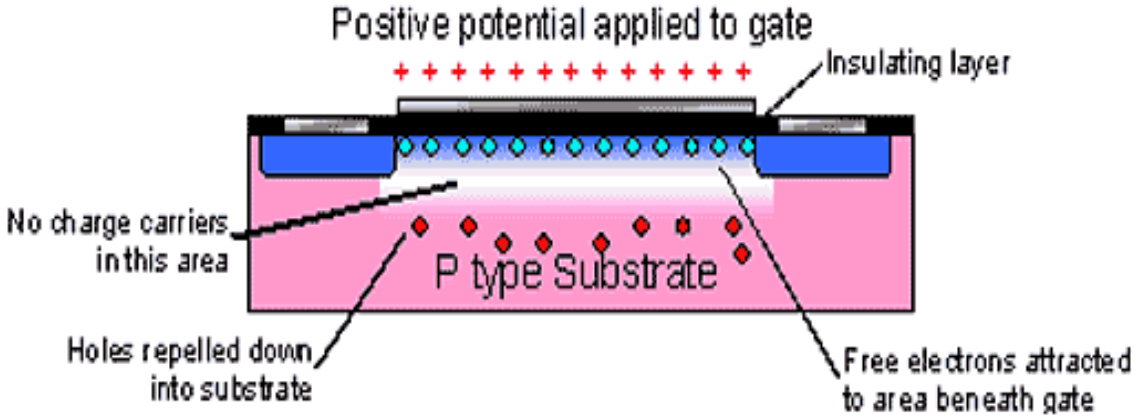
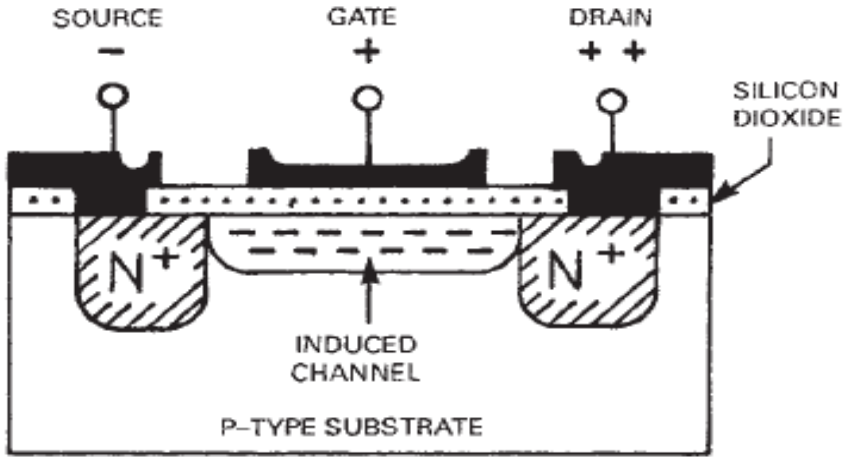


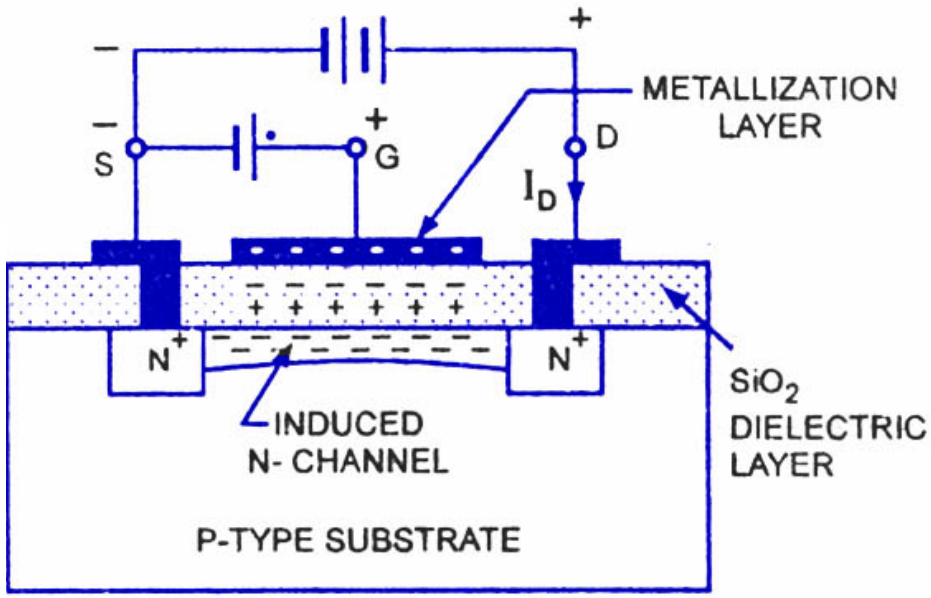
Figure 4.4 (a) NMOS transistor structure; (b) cross section; and (c) circuit symbol.



N-Channel E-MOSFET Structure







Operation of N-Channel E-MOSFET

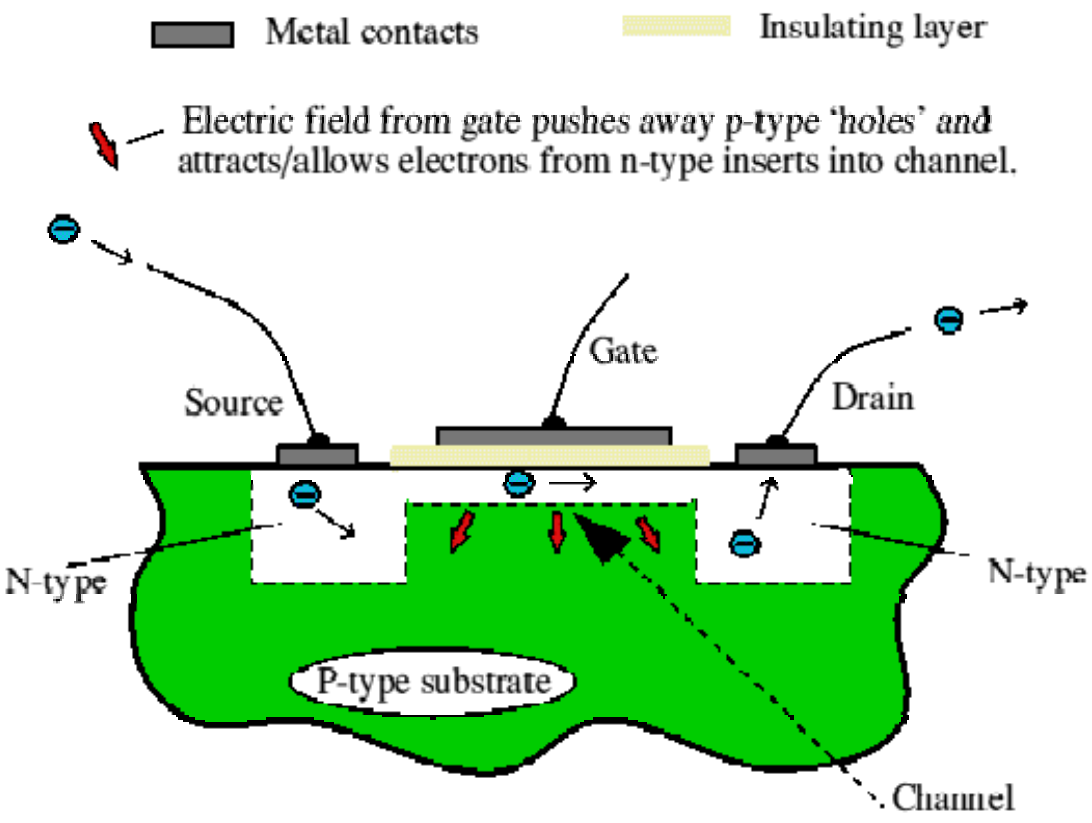


Figure 9.4 N-channel enhancement mode MOSFET.

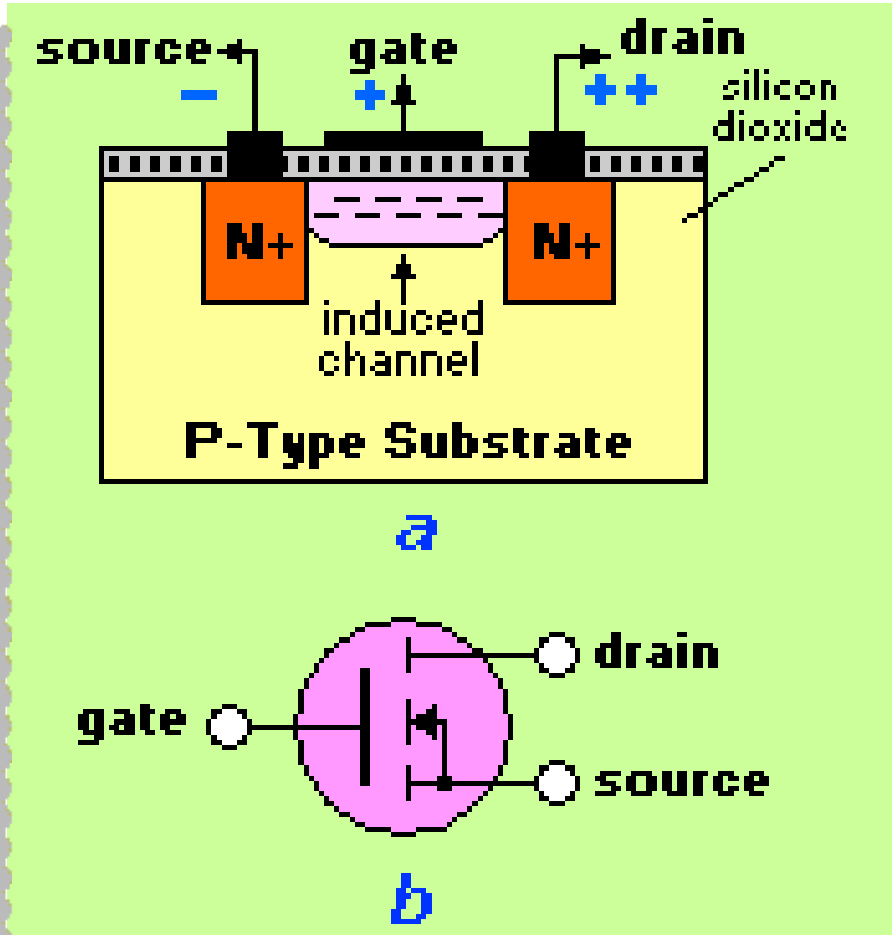
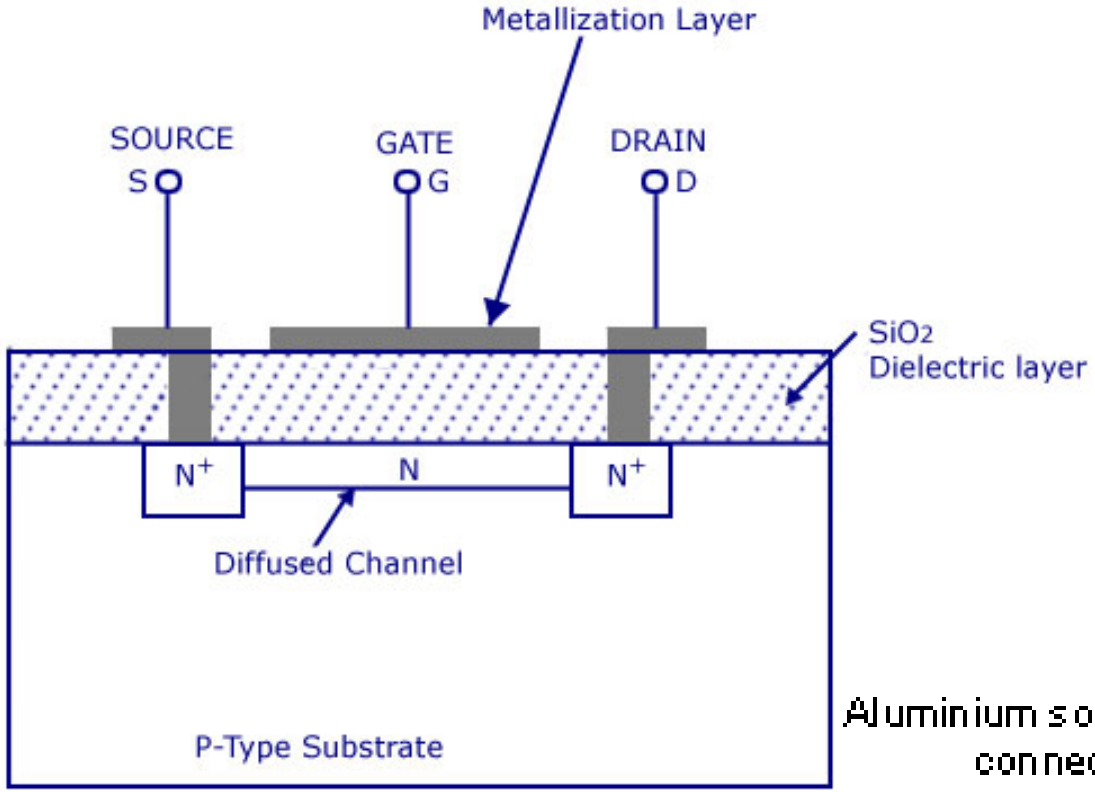
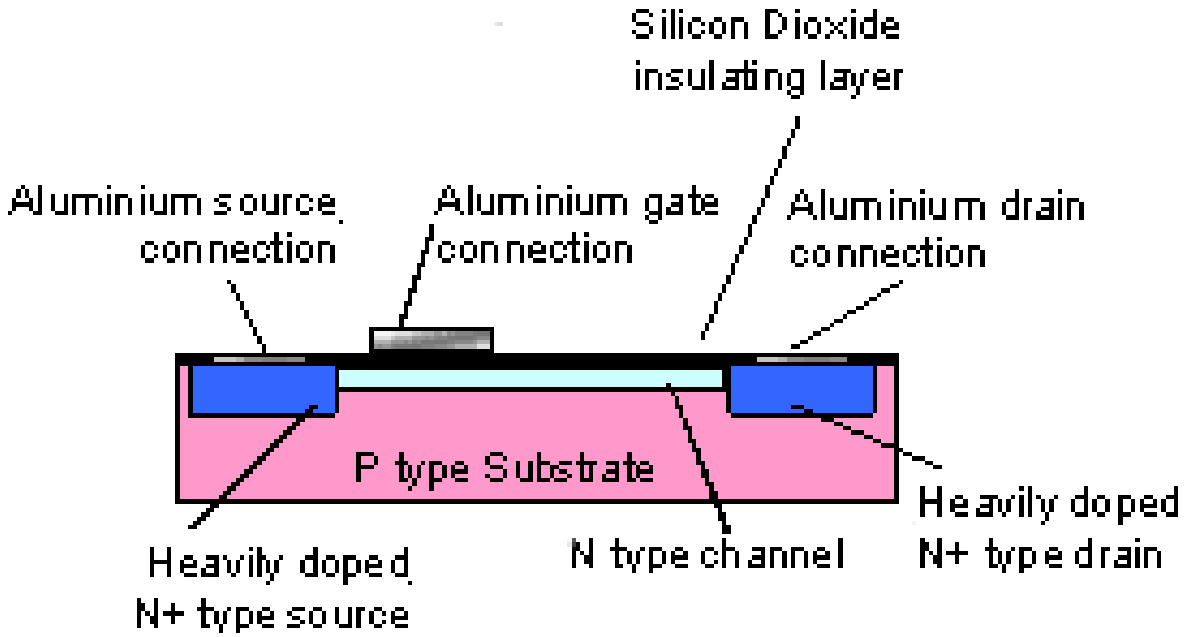
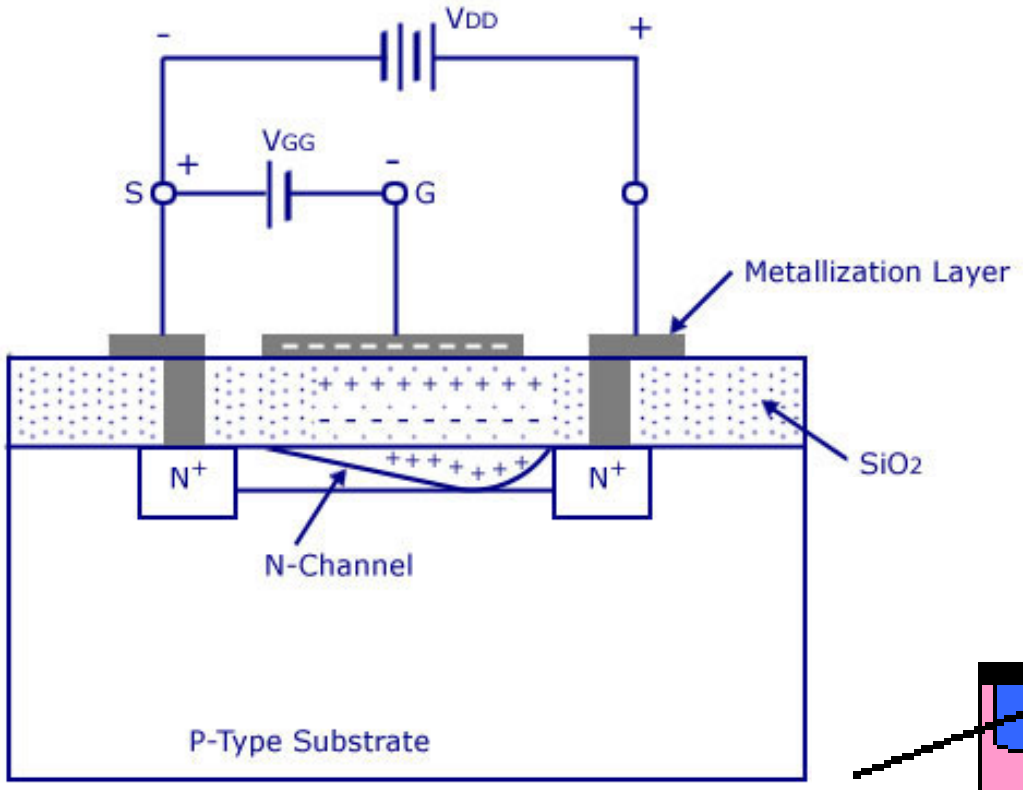


Fig.1 – N-Channel, enhancement-mode planar MOSFET shown in section view (a), and its standard schematic symbol (b).

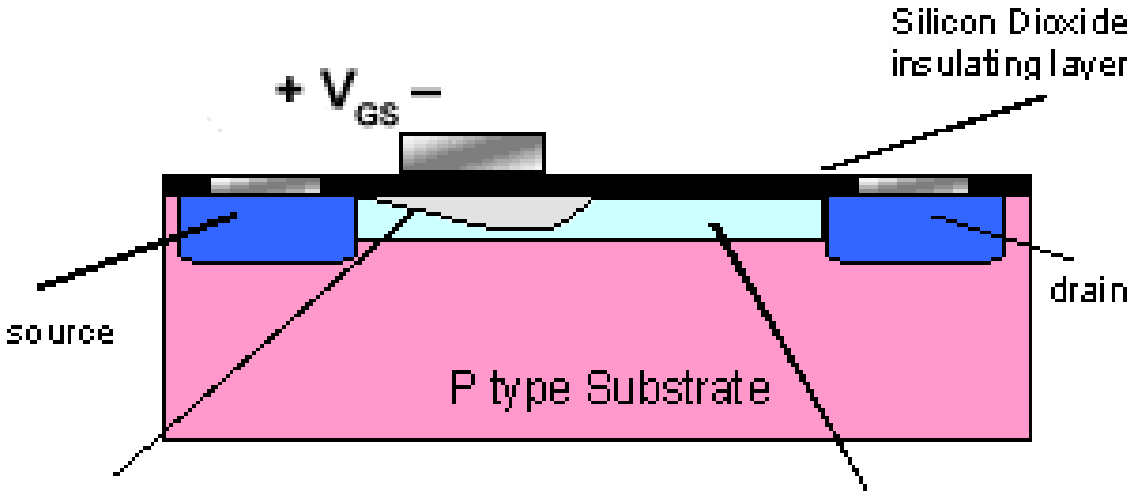


N-Channel DE-MOSFET Structure

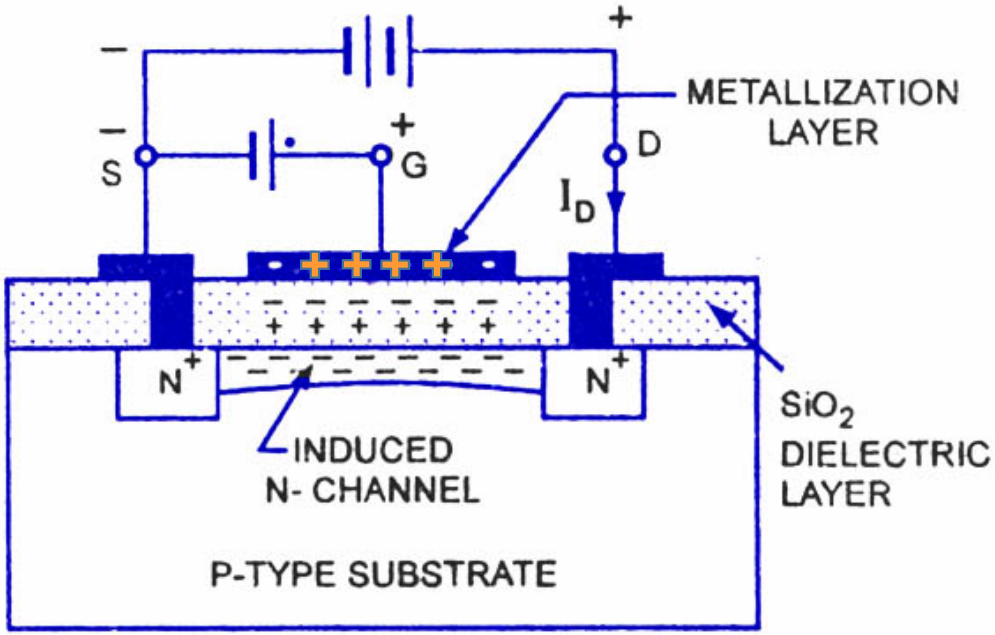




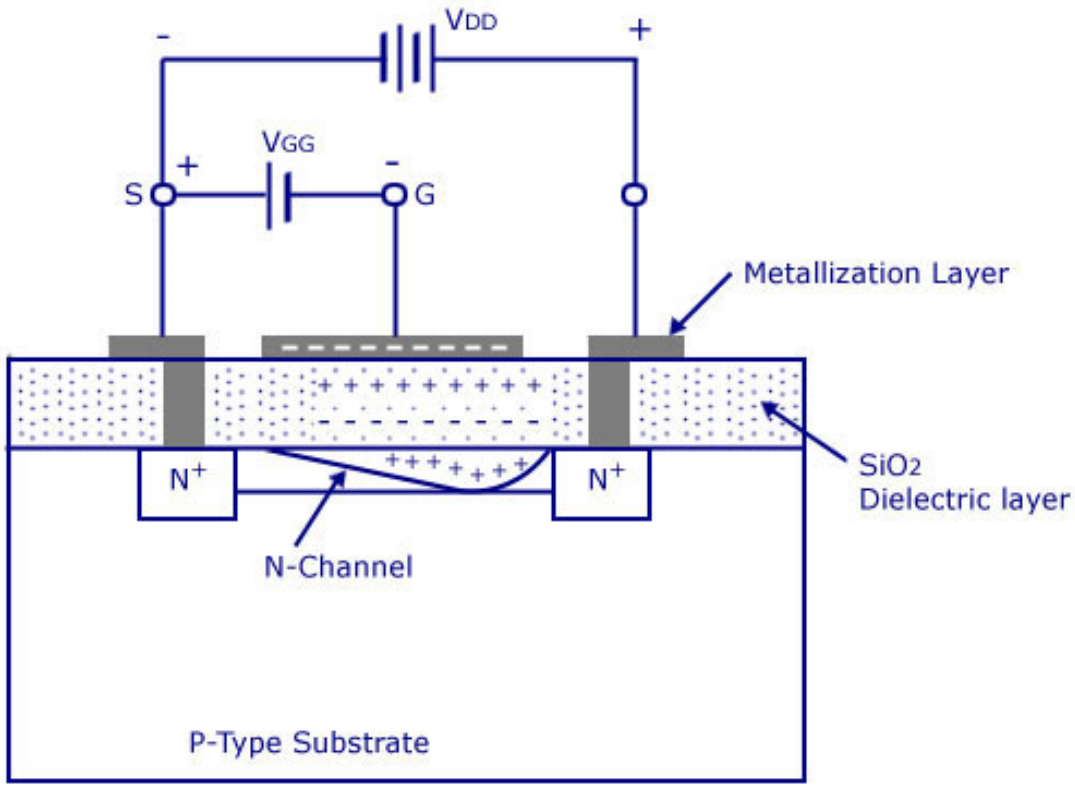
Depletion Mode Operation



As the gate is made more negative than the source, a depletion region is created in the N type channel, reducing conduction between source & drain.

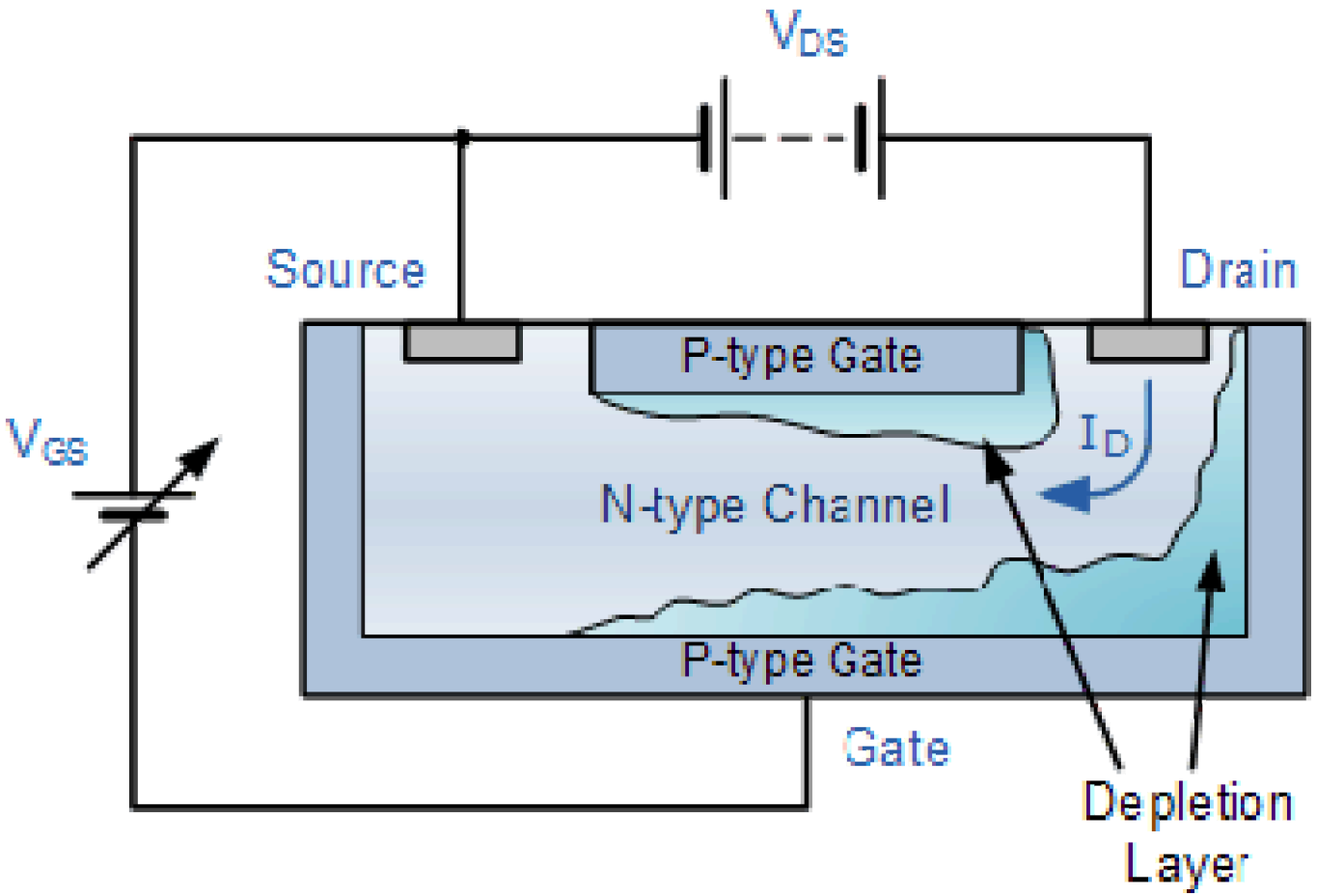


Operation of N-Channel E-MOSFET



Depletion Mode Operation

www.CircuitsToday.com


V_{DS}
Source
Drain
P-type Gate
I_D
V_{GS}
N-type Channel
P-type Gate
Gate
Depletion
Layer

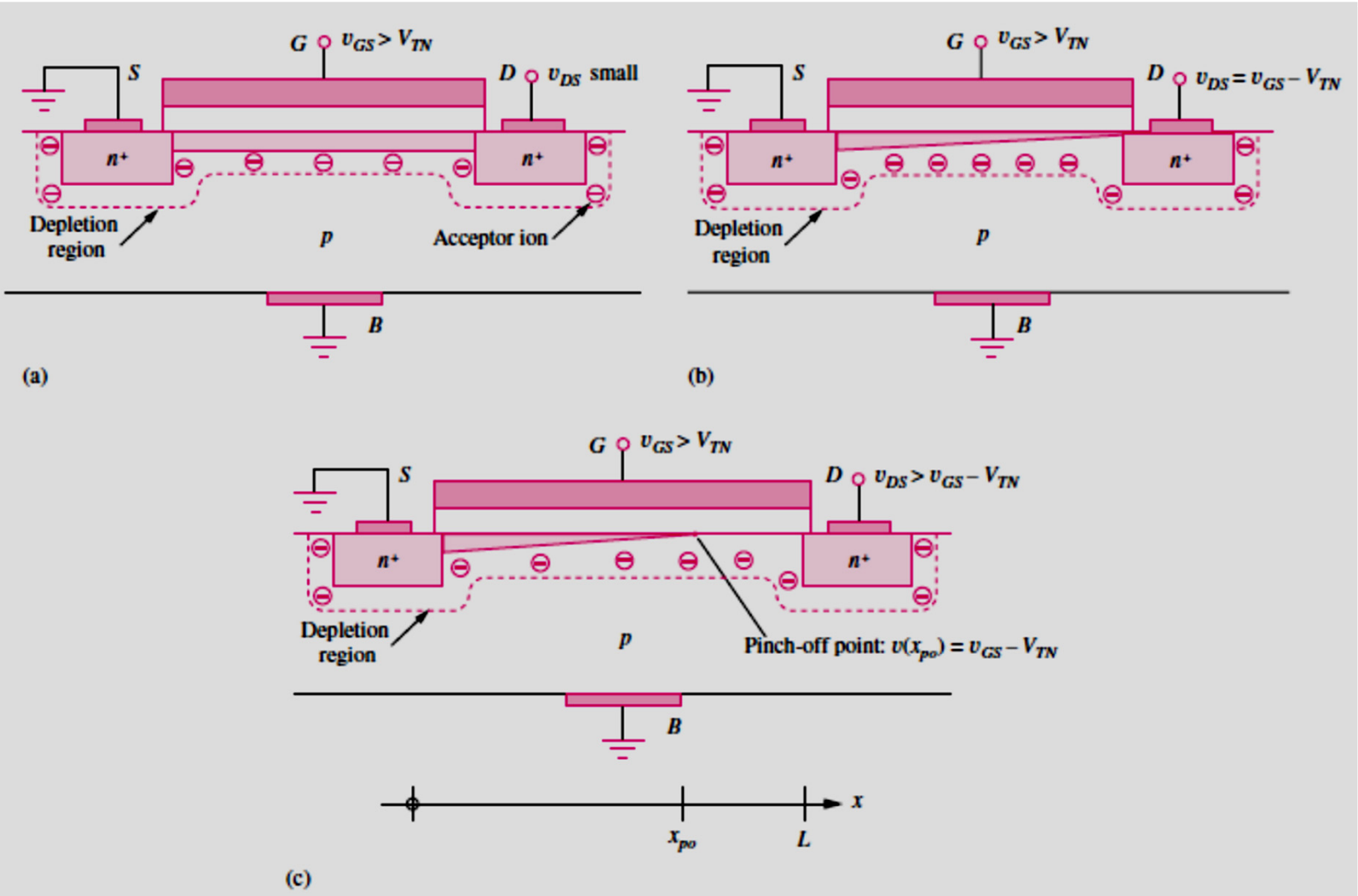
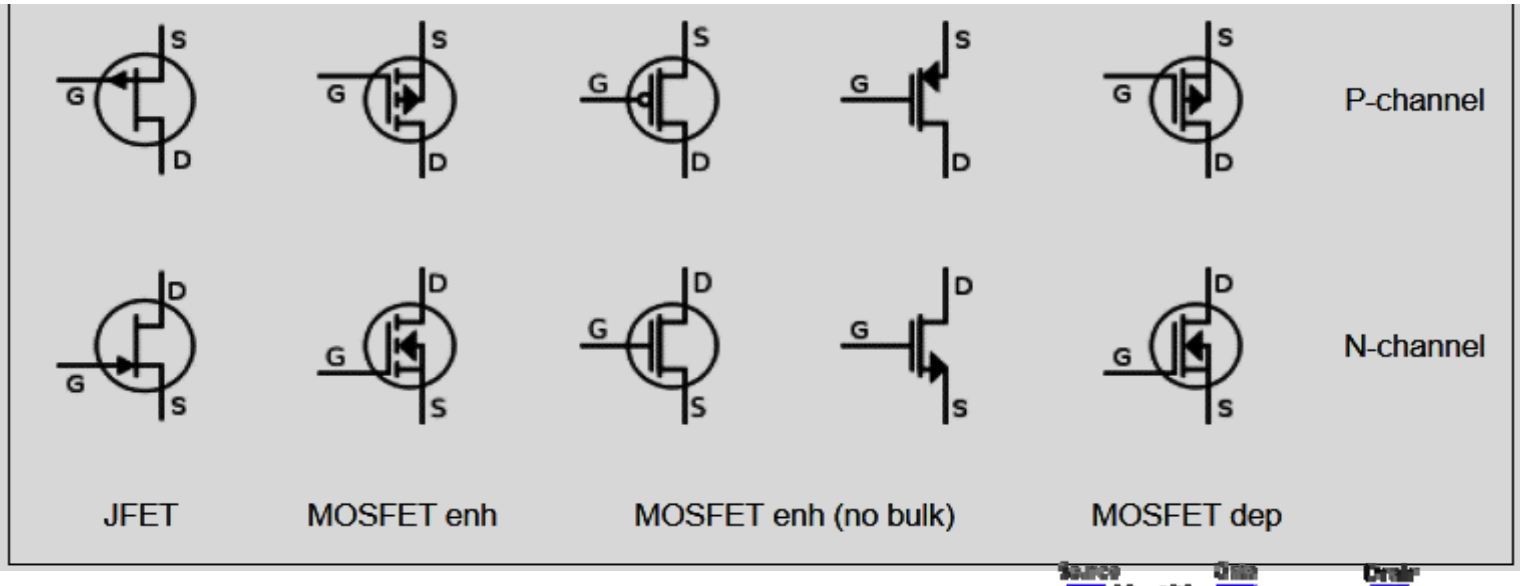
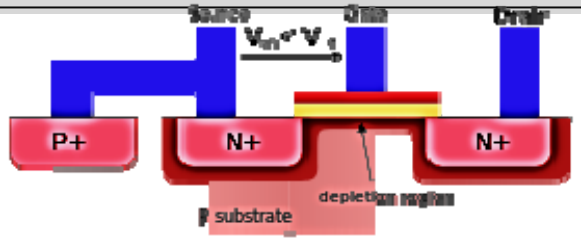
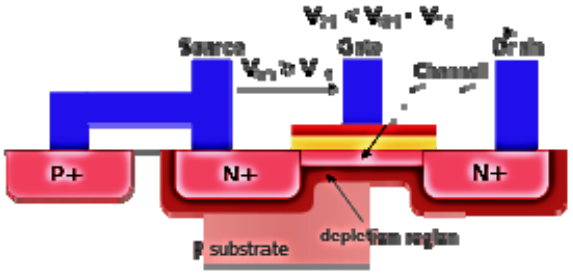


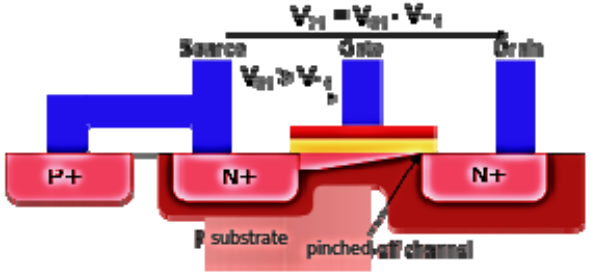
Figure 4.9 (a) MOSFET in the linear region. (b) MOSFET with channel just pinched off at the drain. (c) Channel pinch-off for $v_{DS} > v_{GS} - V_{TN}$.



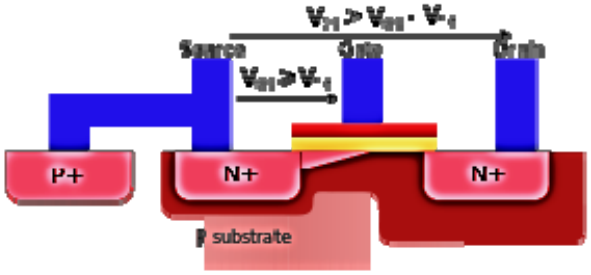




Linear operating region (ohmic mode)



Saturation mode at point of pinch-off

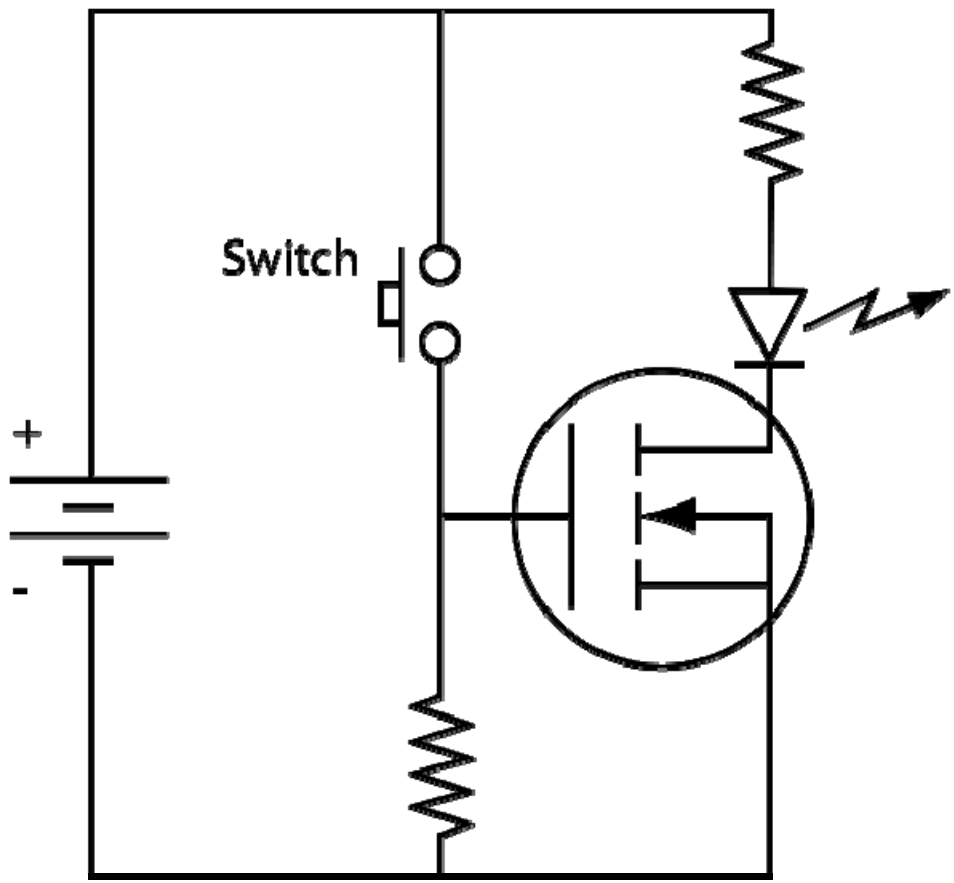


Saturation mode

A MISFET is a metal–insulator–semiconductor field-effect transistor.

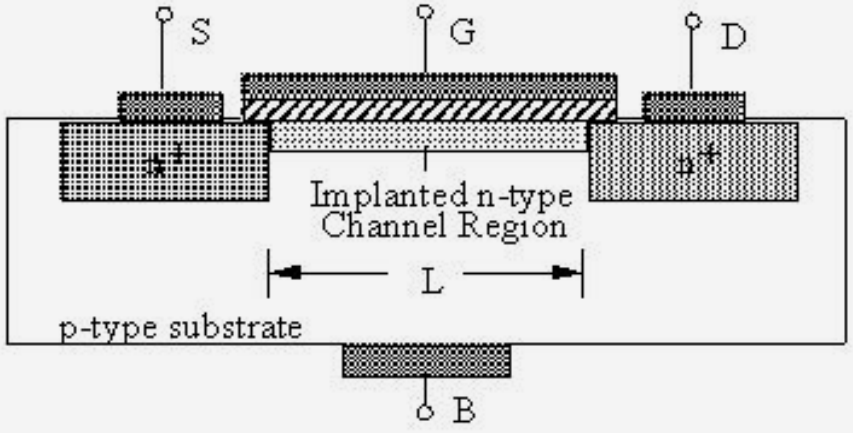
MISFET is a more general term than MOSFET and a synonym to insulated gate field-effect transistor (IGFET).

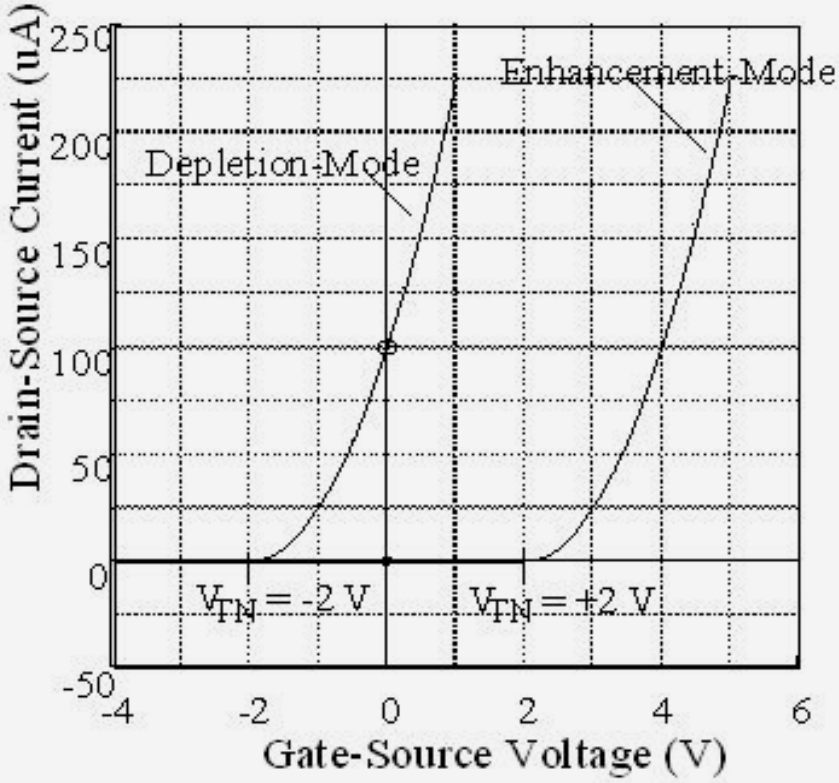
All MOSFETs are MISFETs, but not all MISFETs are MOSFETs.

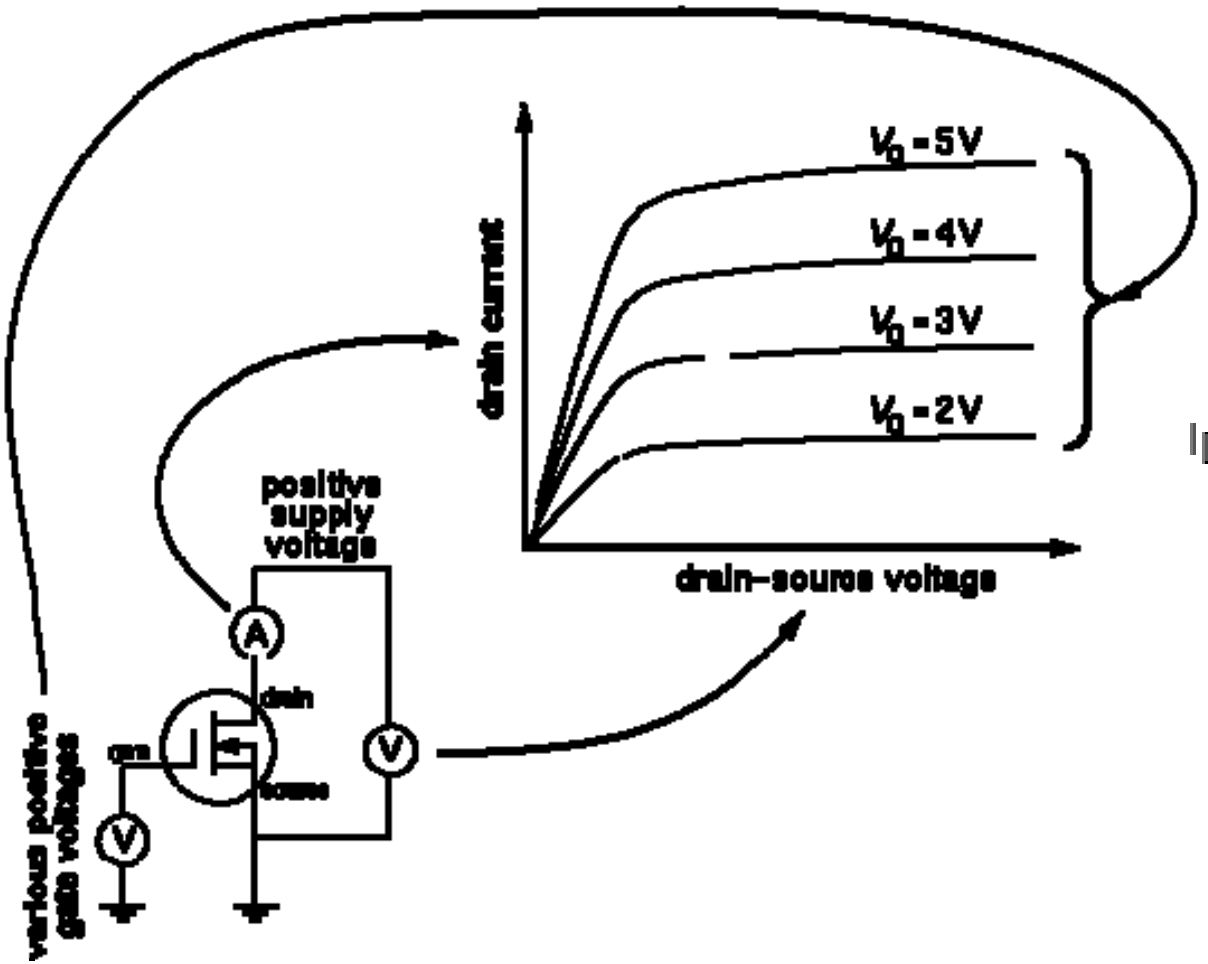


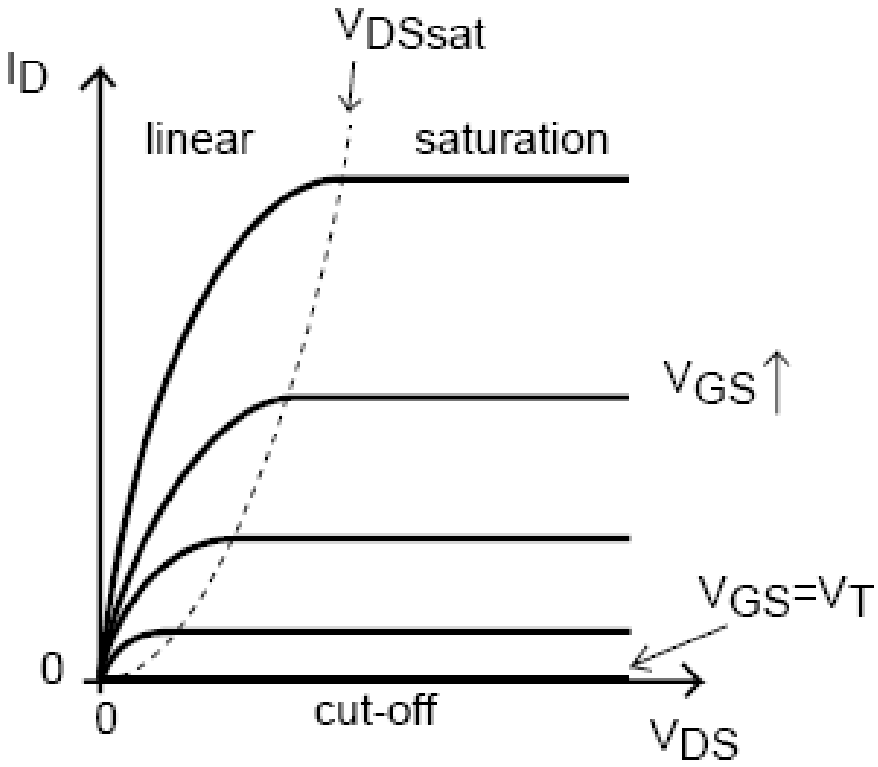
Transfer Characteristics and Depletion Mode MOSFET

- Transfer characteristics: plot of drain current versus gate-source voltage for a fixed drain-source voltage
- If threshold voltage of NMOS transistor negative → depletion mode MOSFET (there exists an implanted n-type channel region)



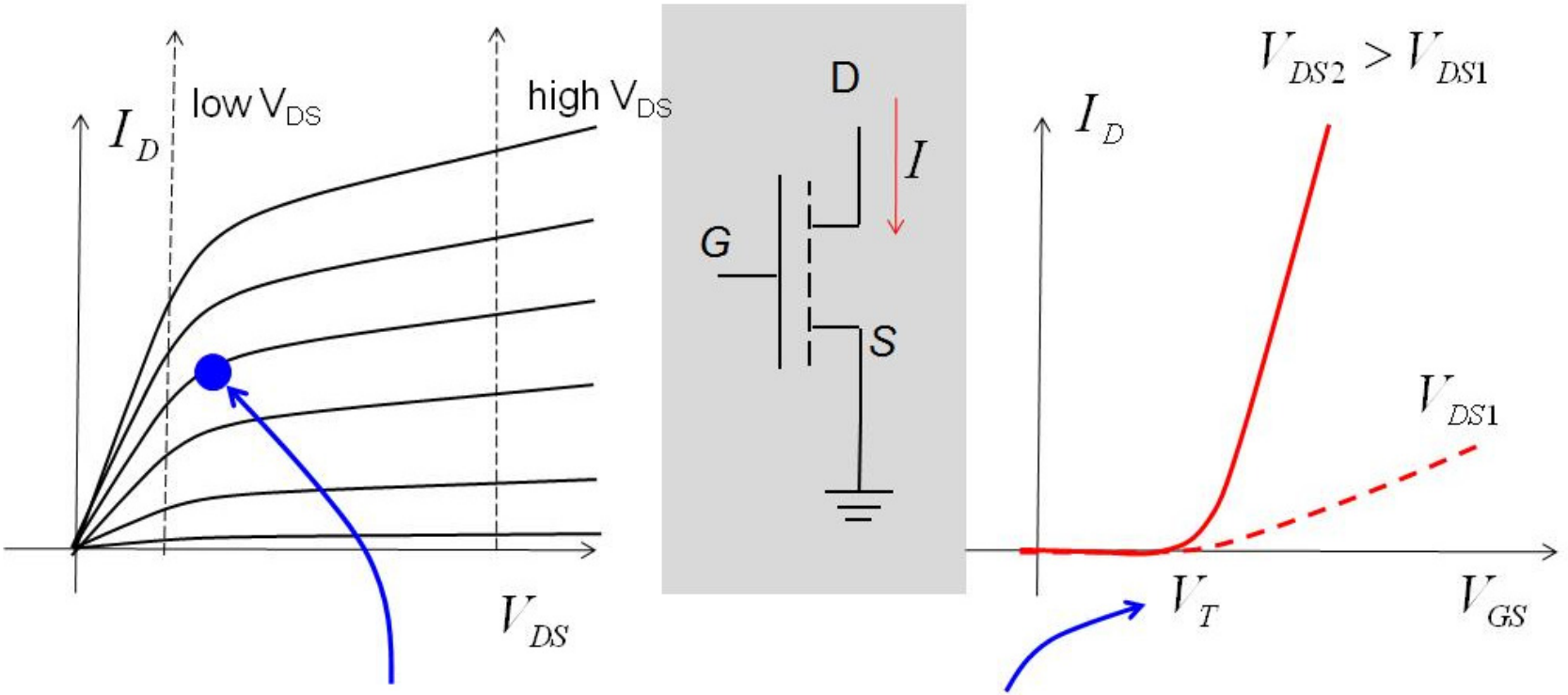



V_g = 5V
V_g = 4V
V_g = 3V
V_g = 2V
drain current
drain-source voltage
positive supply voltage
various positive gate voltages
A
V
drain
gate
source


V_{DSsat}
I_D
linear
saturation
V_{GS} ↑
$V_{GS}=V_T$
0
0
cut-off
V_{DS}

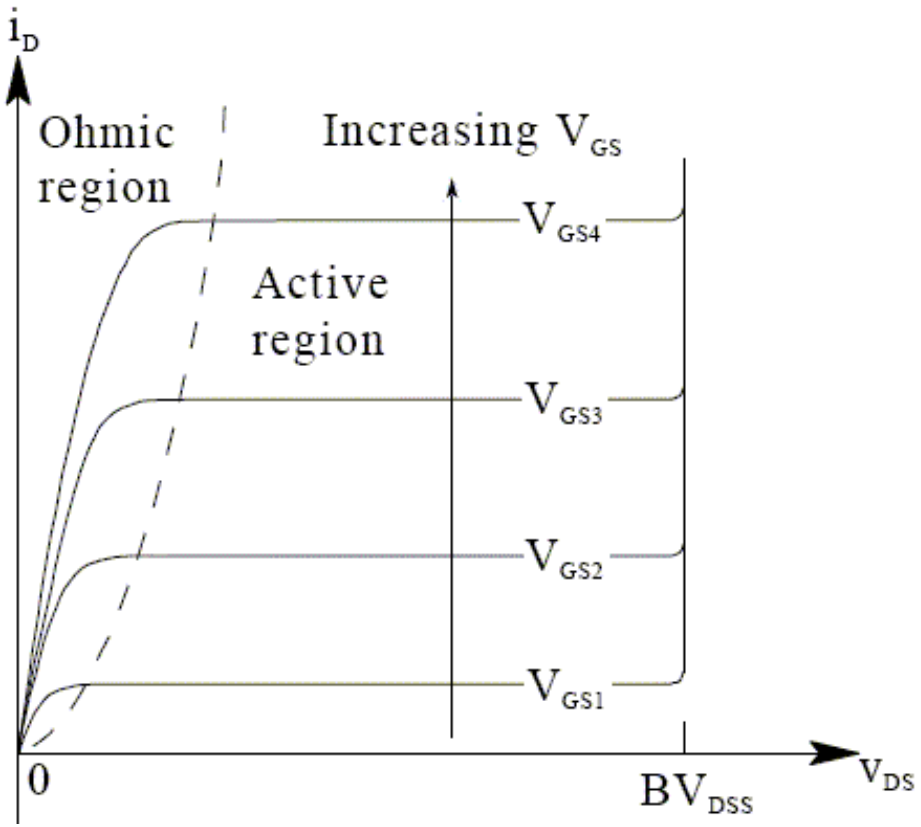
output and transfer characteristics

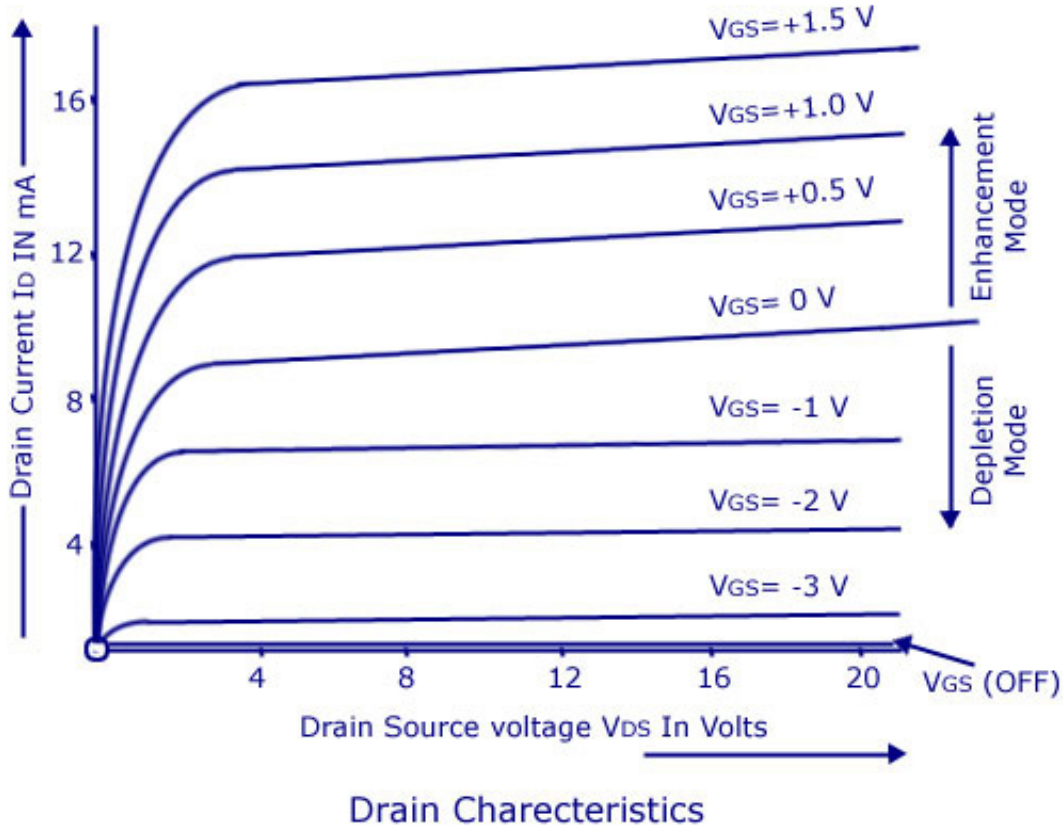
output characteristics



"saturation voltage" V_{DSAT}

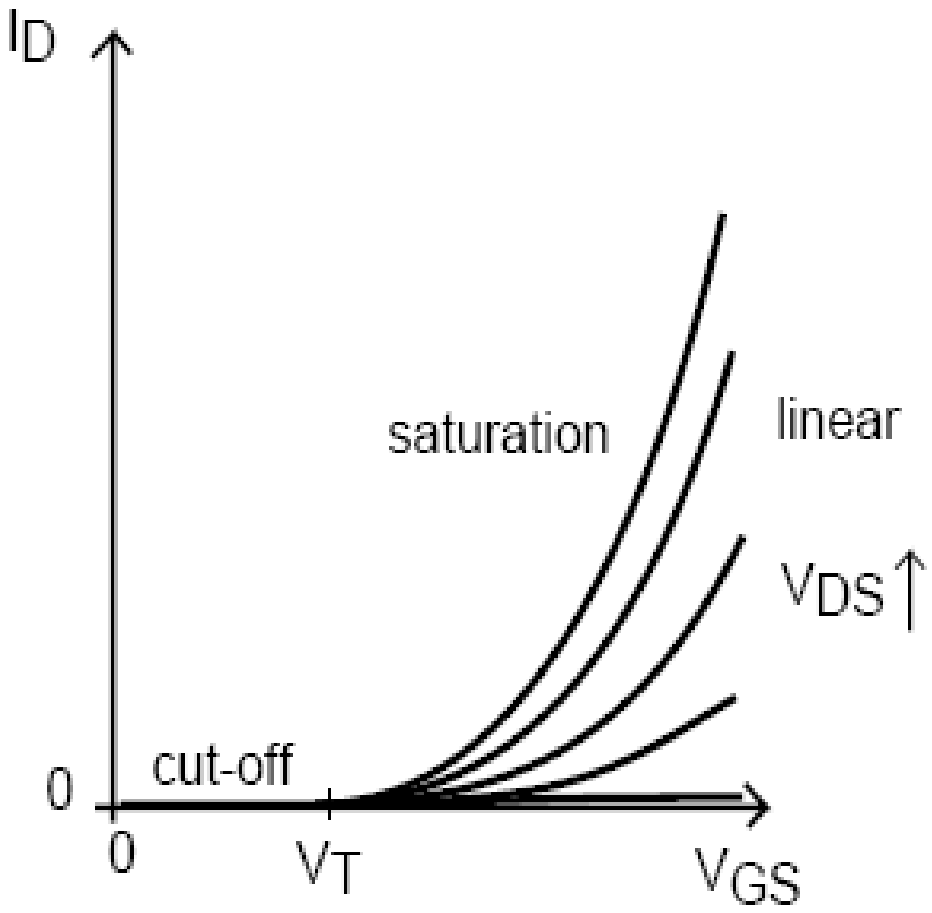
"threshold voltage"

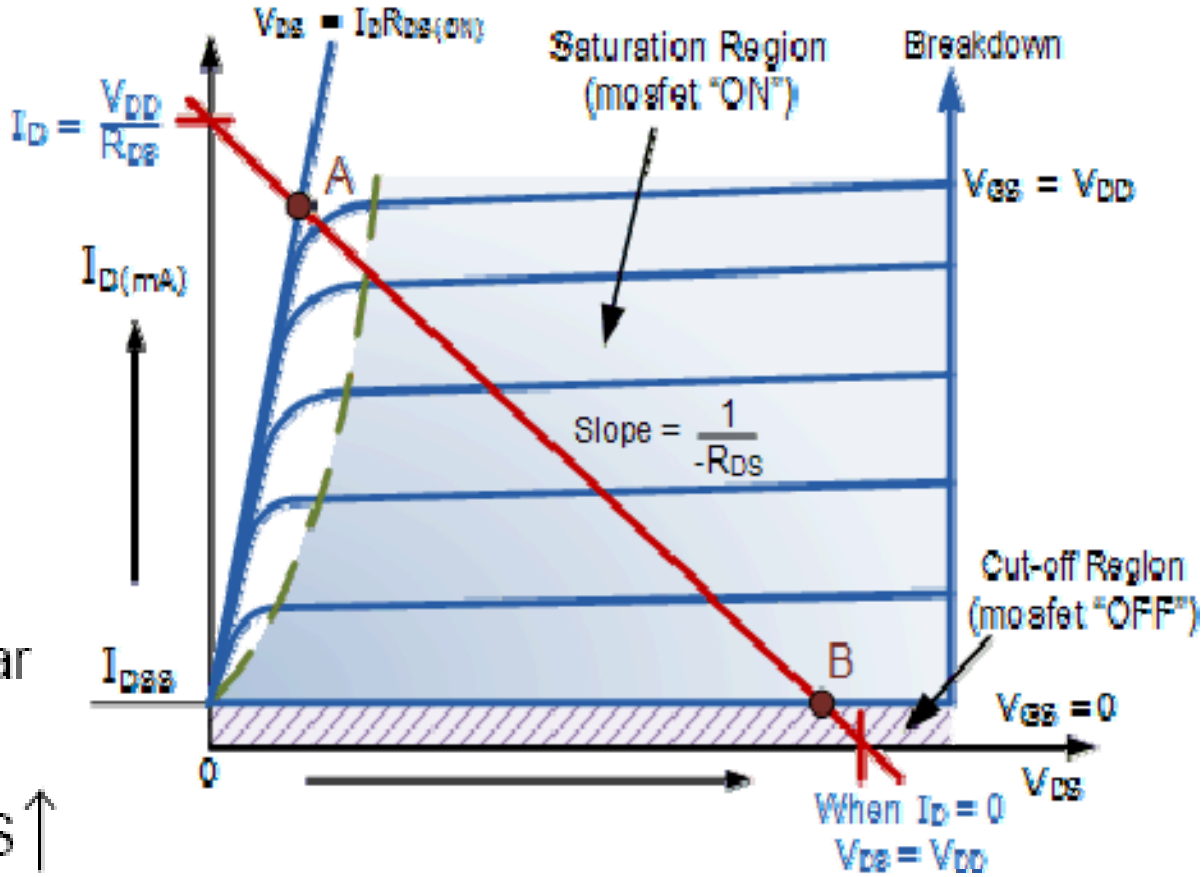


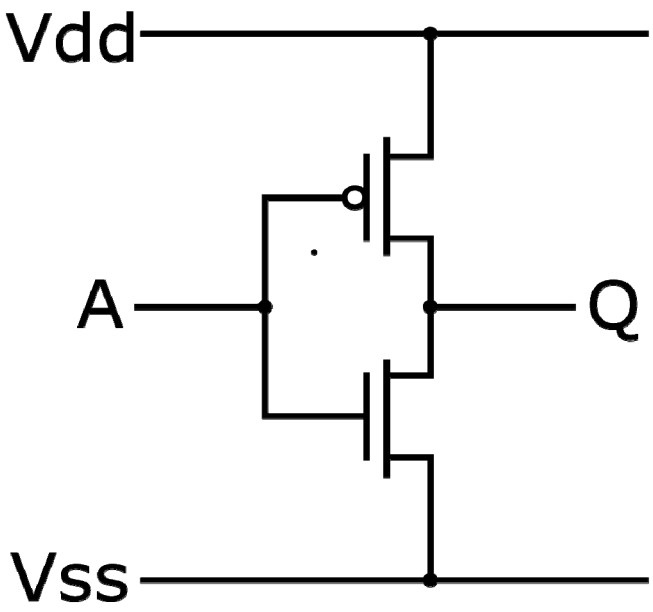


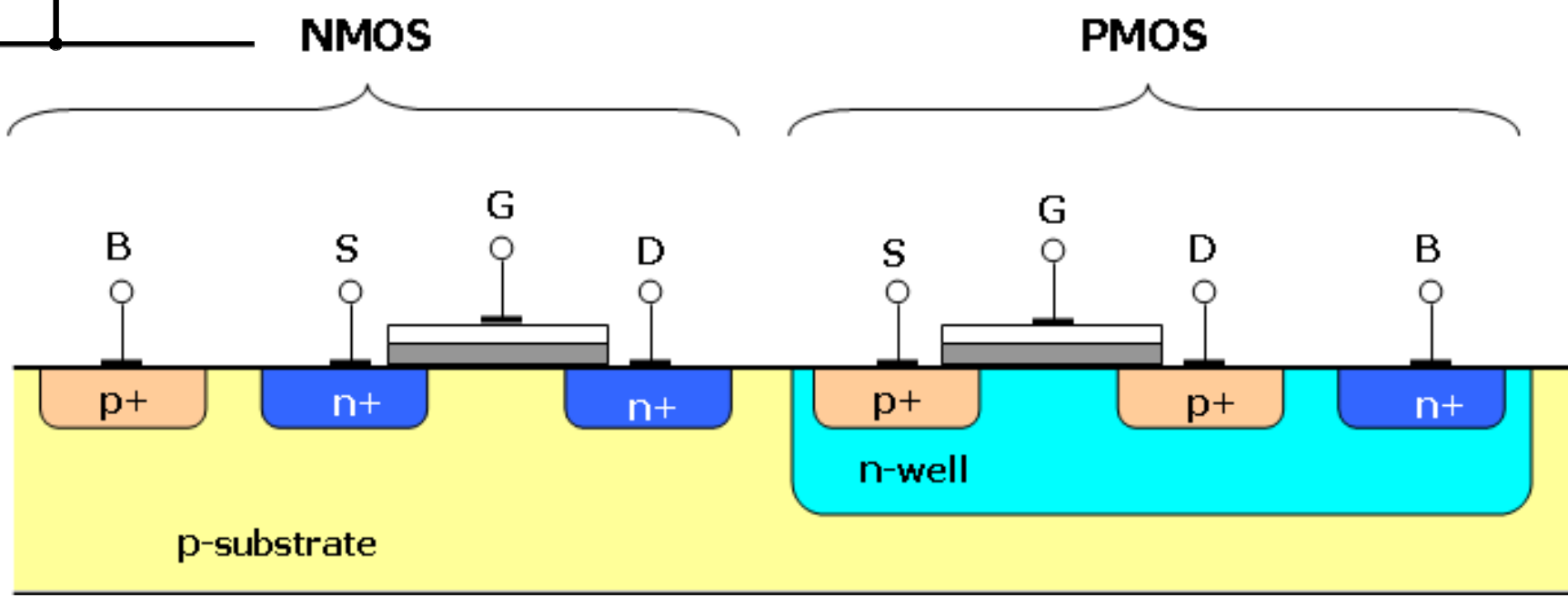
Drain Charecteristics

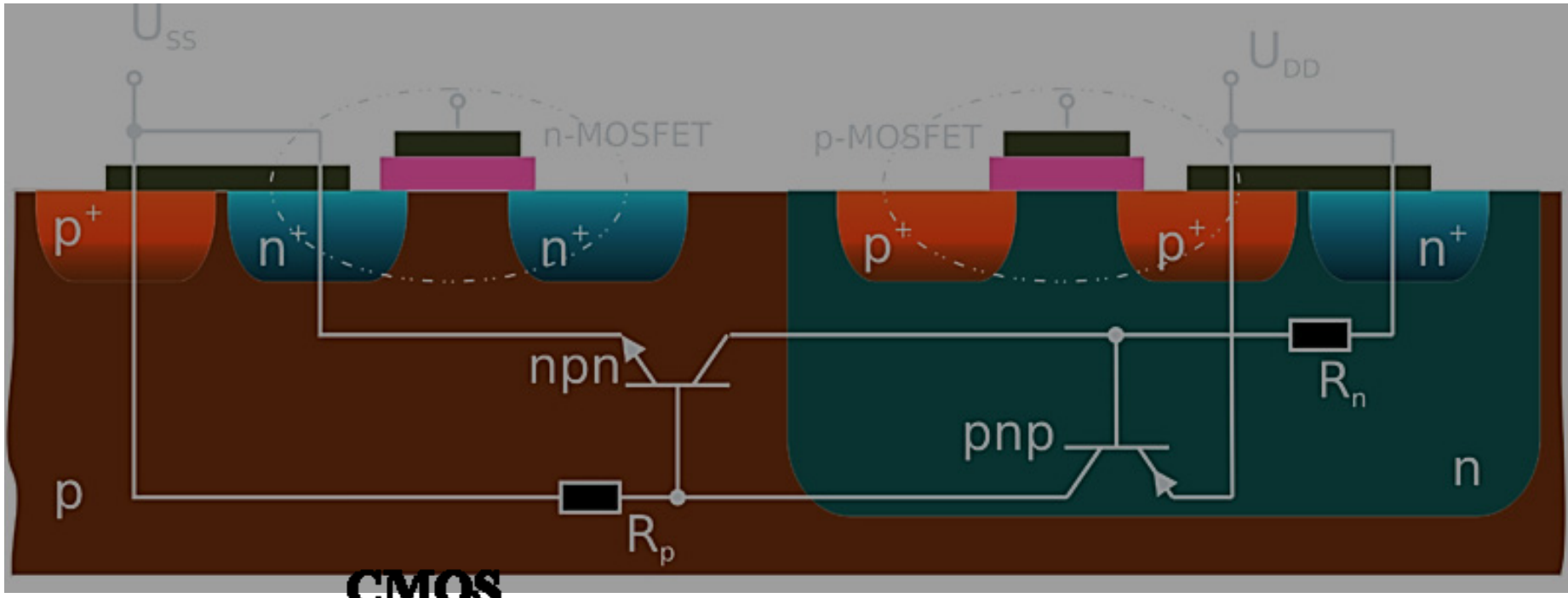
www.circuitsToday.com


I_D
saturation
linear
V_{DS} ↑
cut-off
0
0
V_T
V_{GS}


$V_{DS} = I_D R_{DS(ON)}$
$I_D = \frac{V_{DD}}{R_{DS}}$
Saturation Region
(mosfet "ON")
Breakdown
A
$V_{GS} = V_{DD}$
$I_{D(mA)}$
Slope = $\frac{1}{-R_{DS}}$
Cut-off Region
(mosfet "OFF")
I_{DSS}
B
$V_{GS} = 0$
0
V_{DS}
When $I_D = 0$
$V_{DS} = V_{DD}$

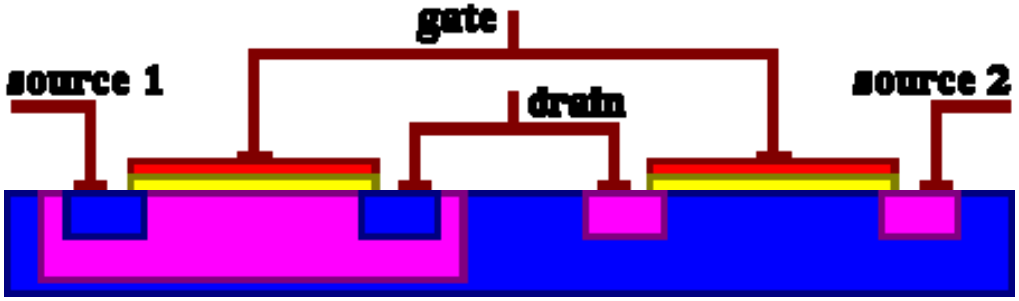

Vdd
A
Q
Vss


NMOS
PMOS
B
S
G
D
S
G
D
B
p+
n+
n+
p+
p+
n+
n-well
p-substrate



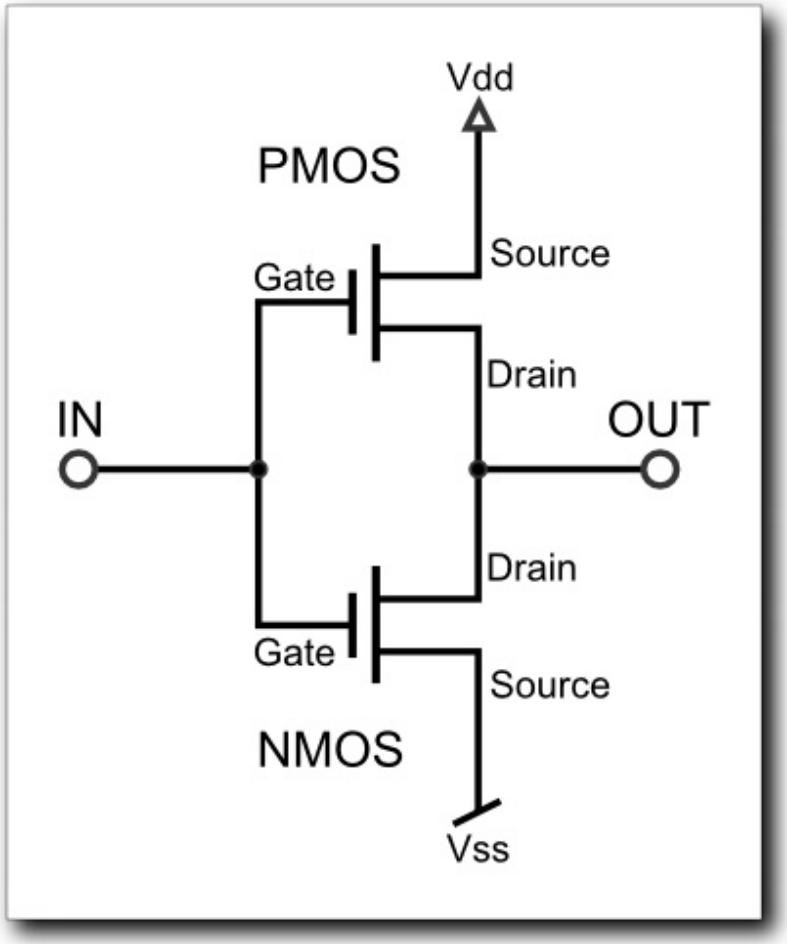
CMOS inverter

metal
oxide (insulator)
n-type semiconductor
p-type semiconductor

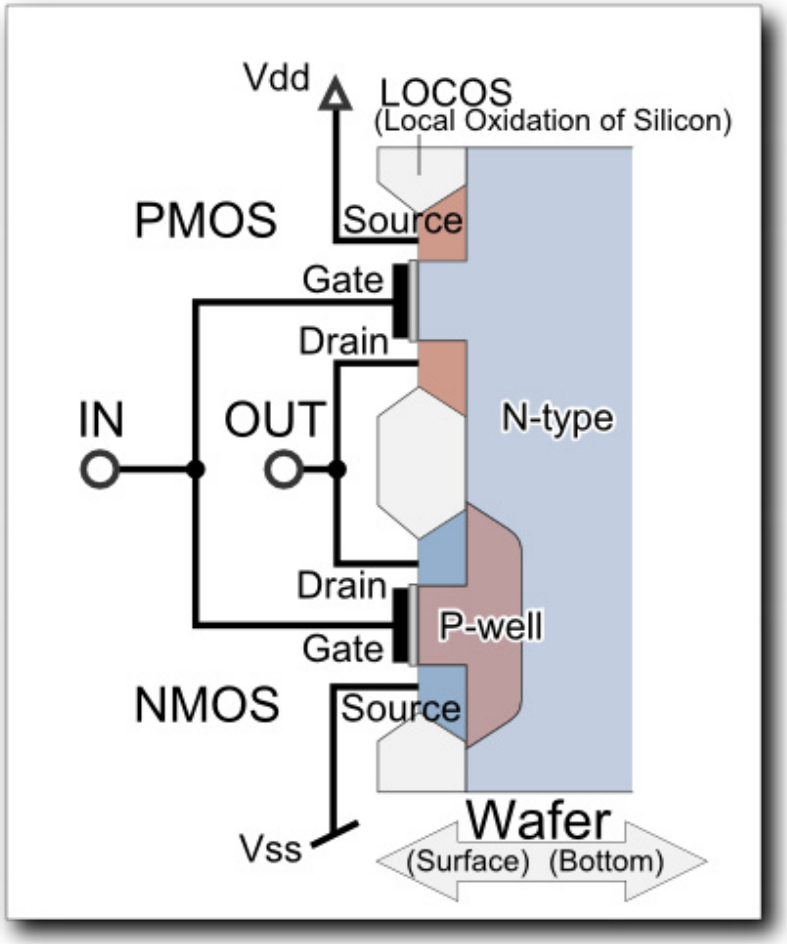


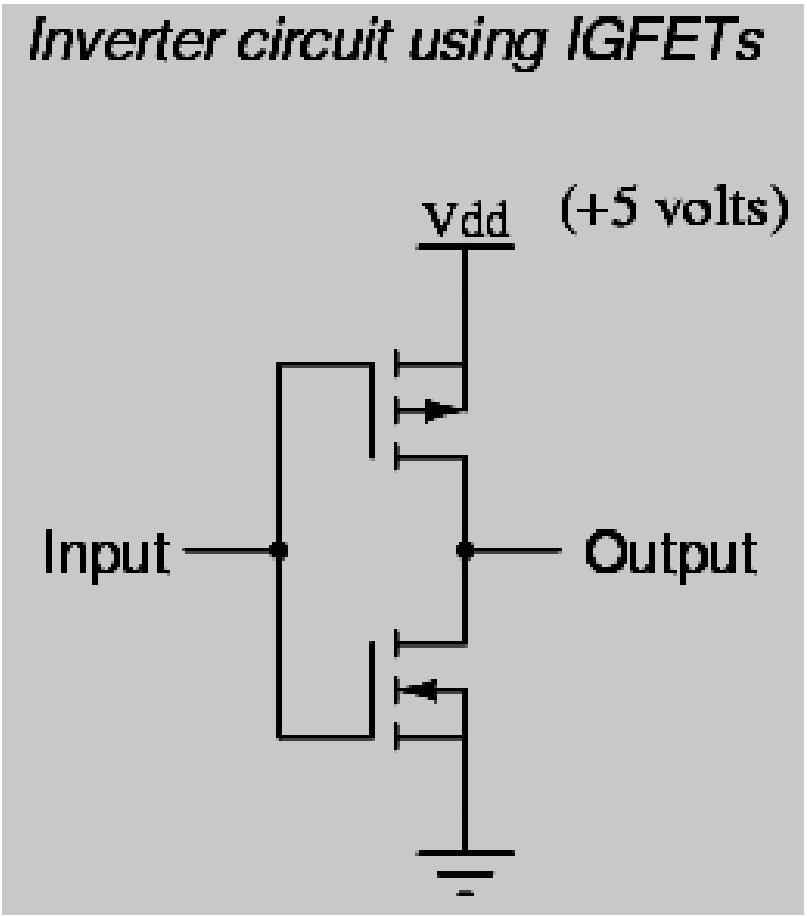
CMOS inverter

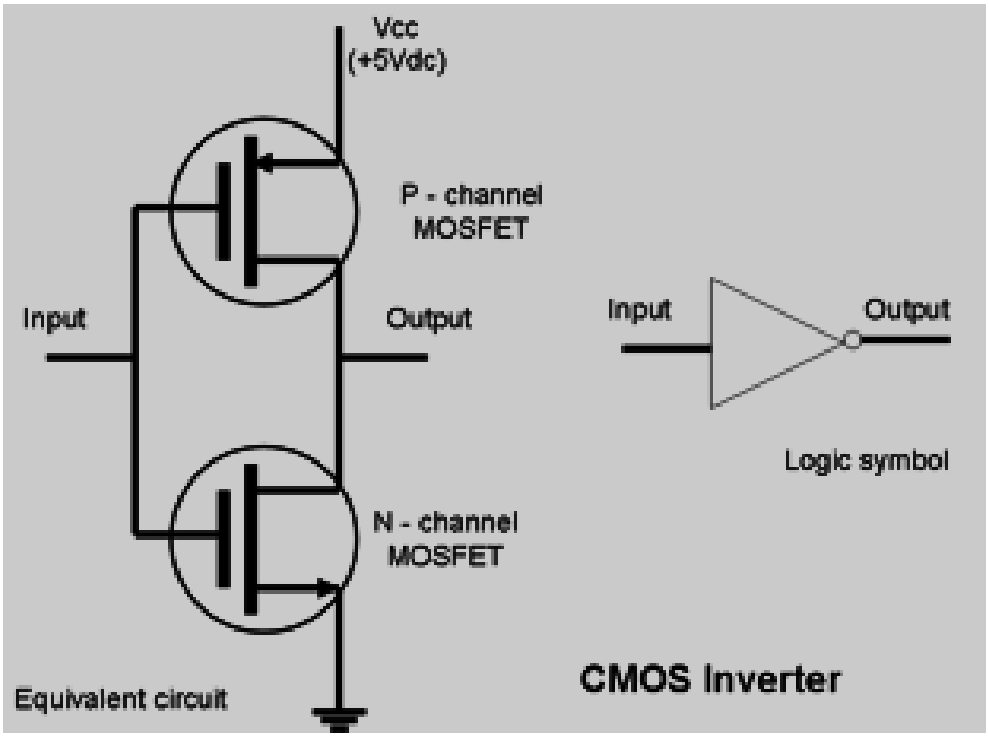
Model chart



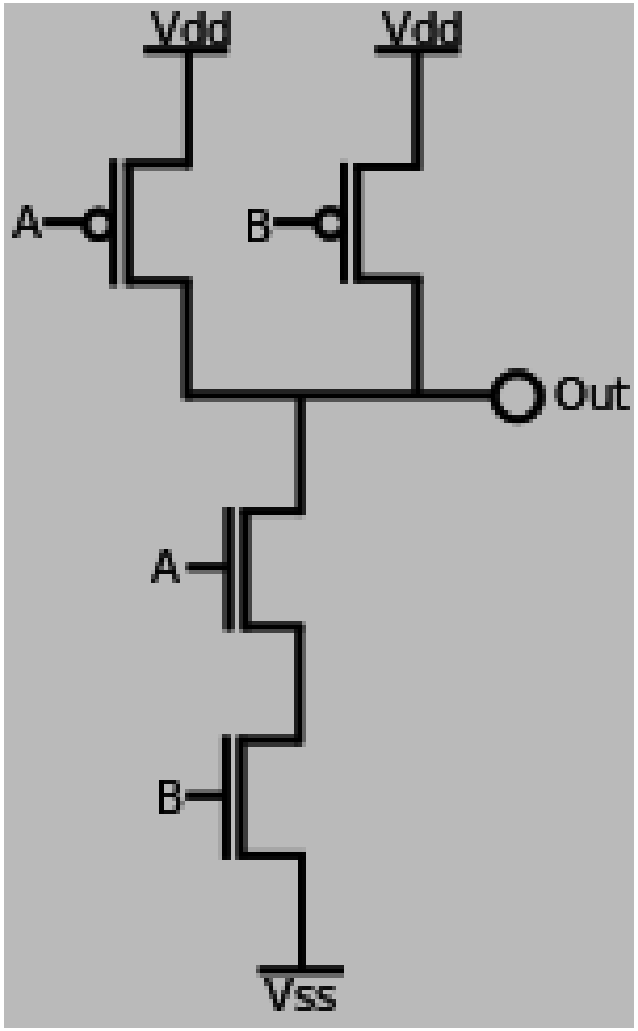
Silicon wafer

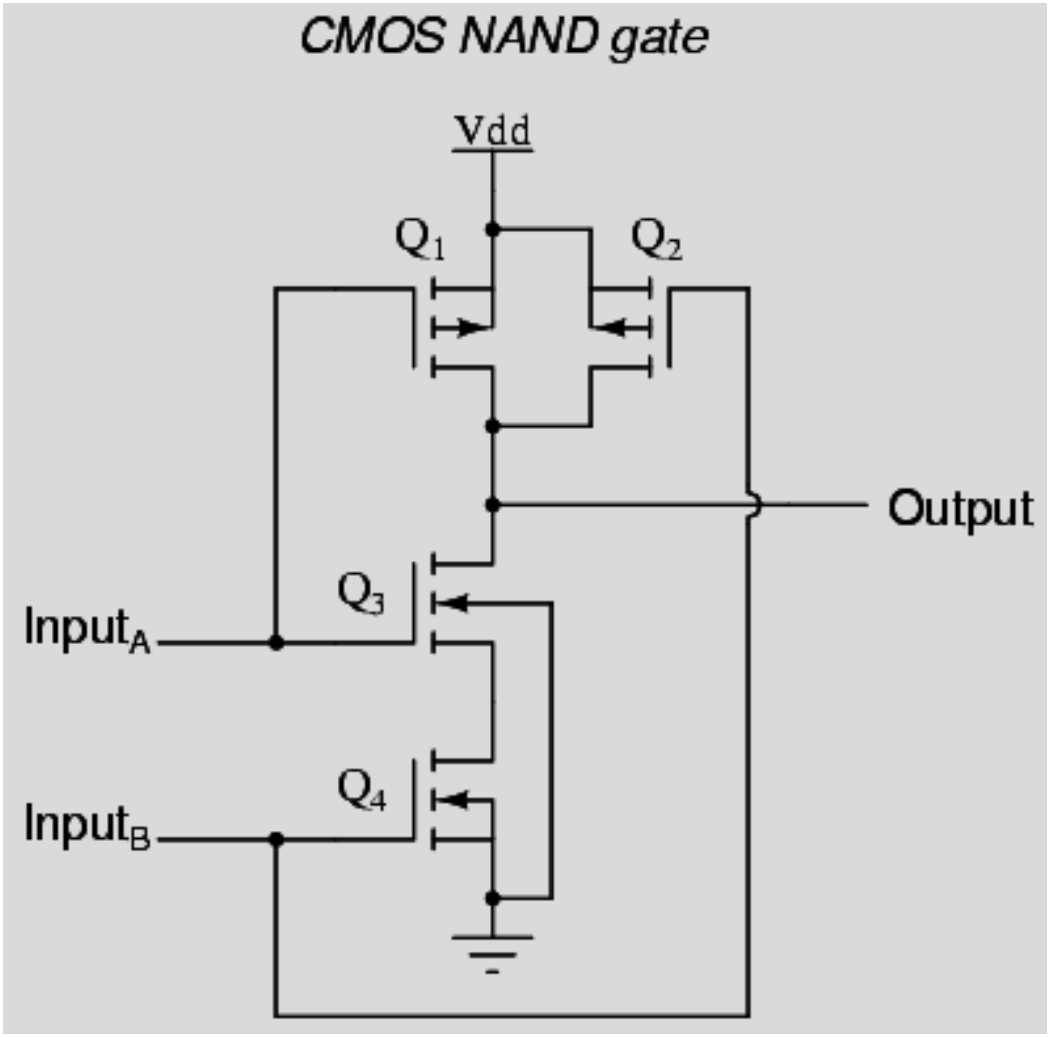


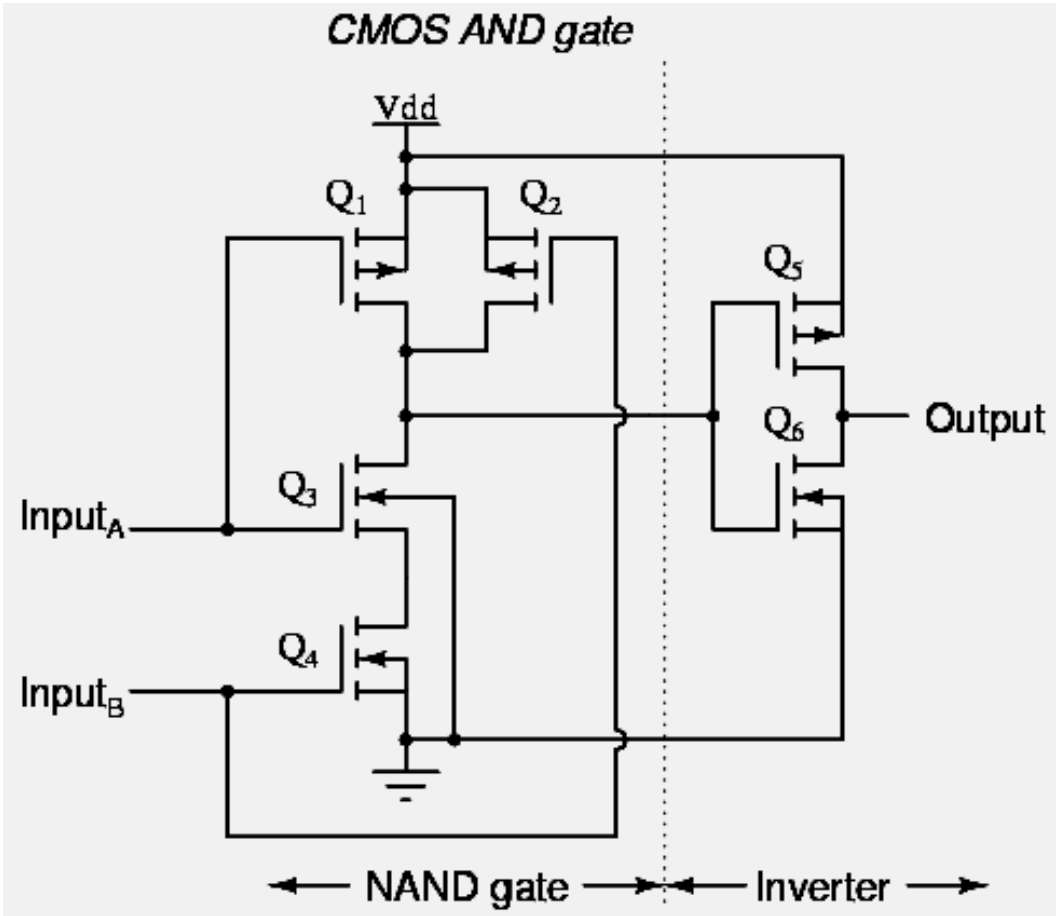


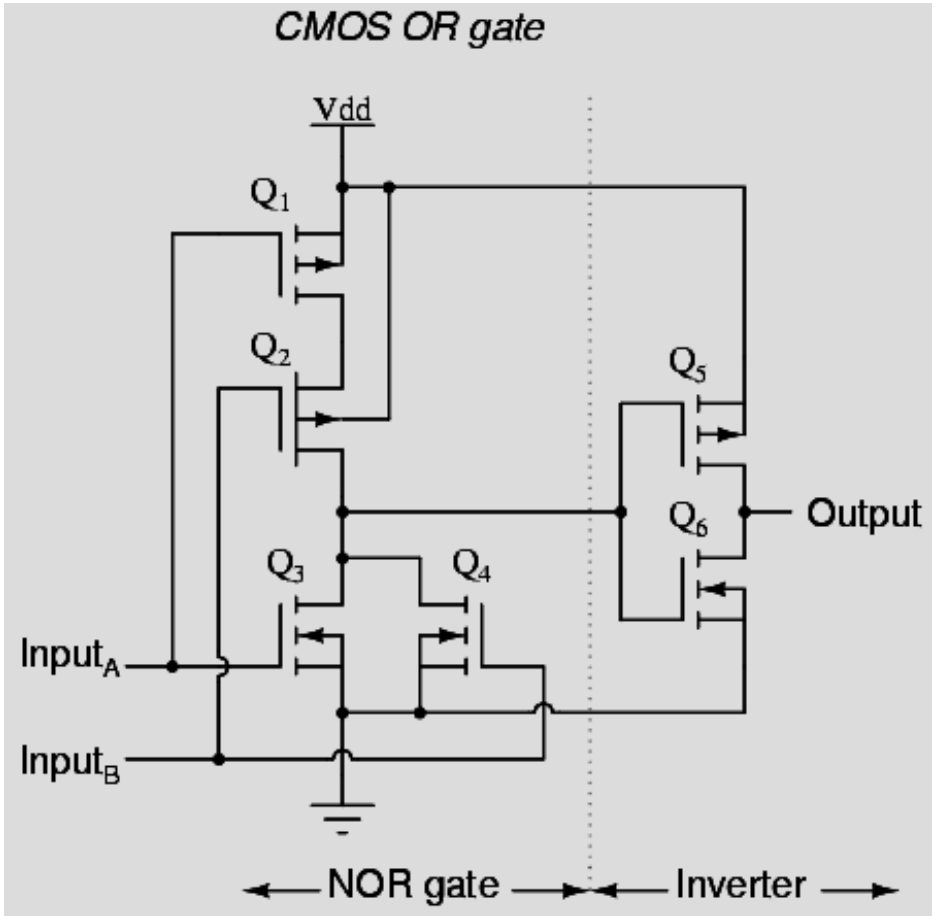


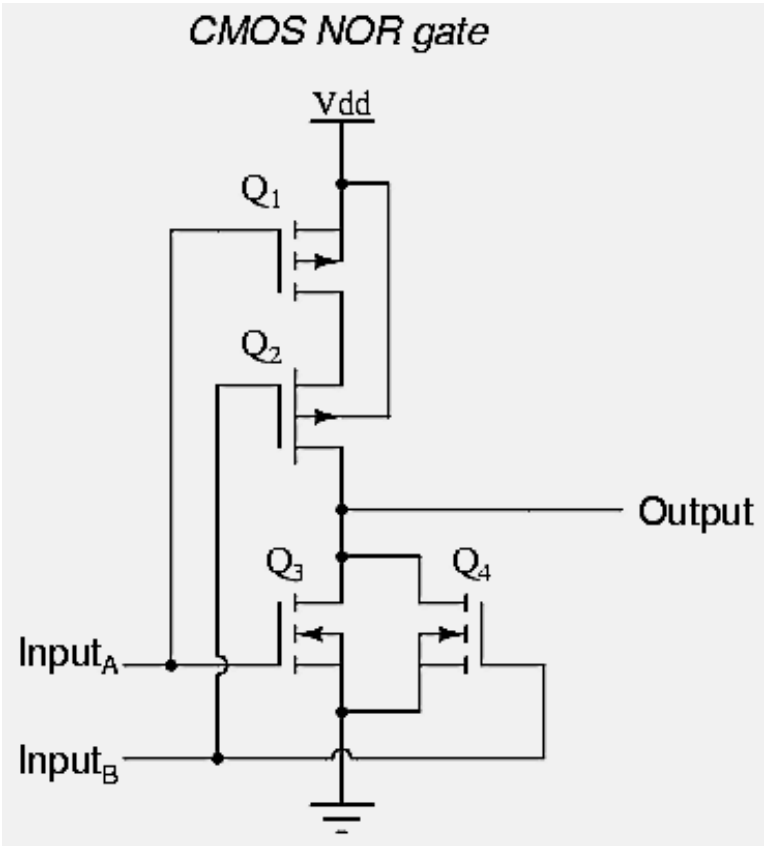
An insulated-gate field-effect transistor or *IGFET*

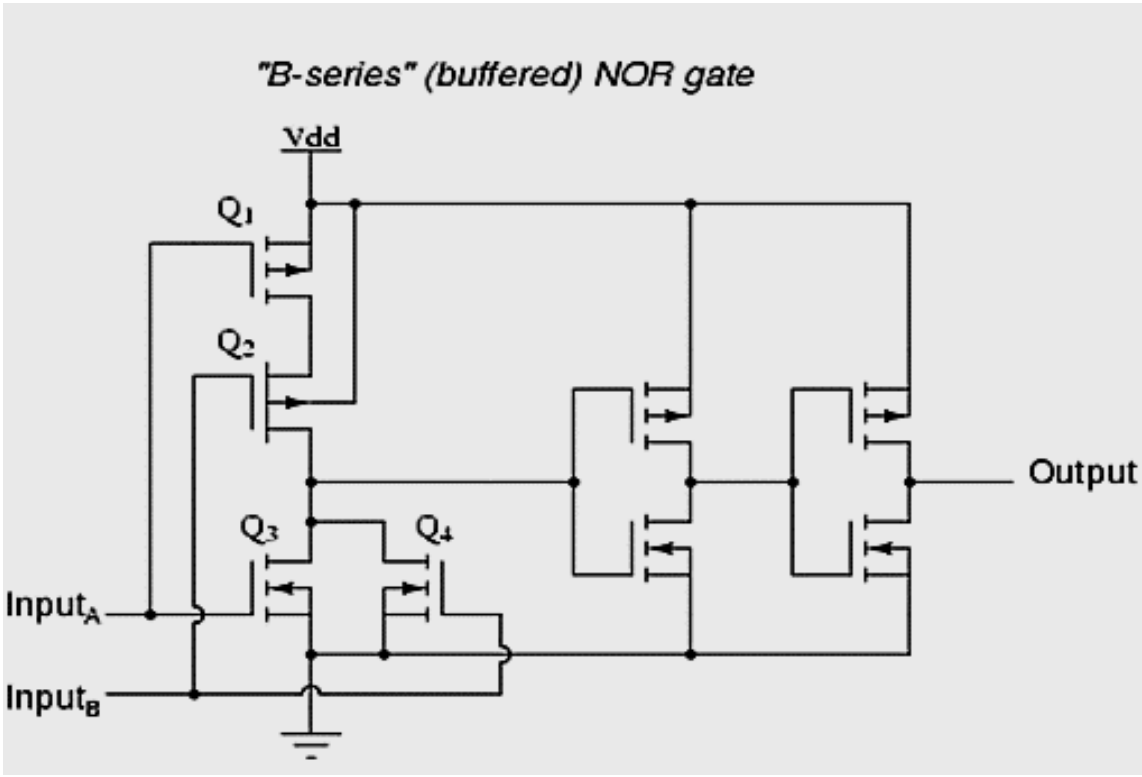

Vdd
Vdd
A
B
Out
A
B
Vss


CMOS NAND gate
Vdd
Q1
Q2
Output
Q3
InputA
Q4
InputB

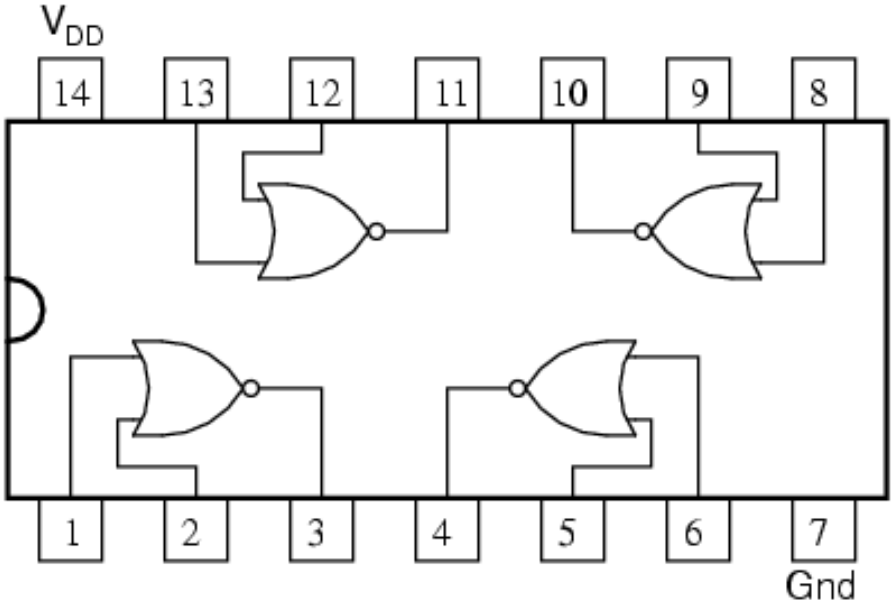

CMOS AND gate
Vdd
Q1
Q2
Q5
Q6
Output
Q3
InputA
Q4
InputB
NAND gate
Inverter

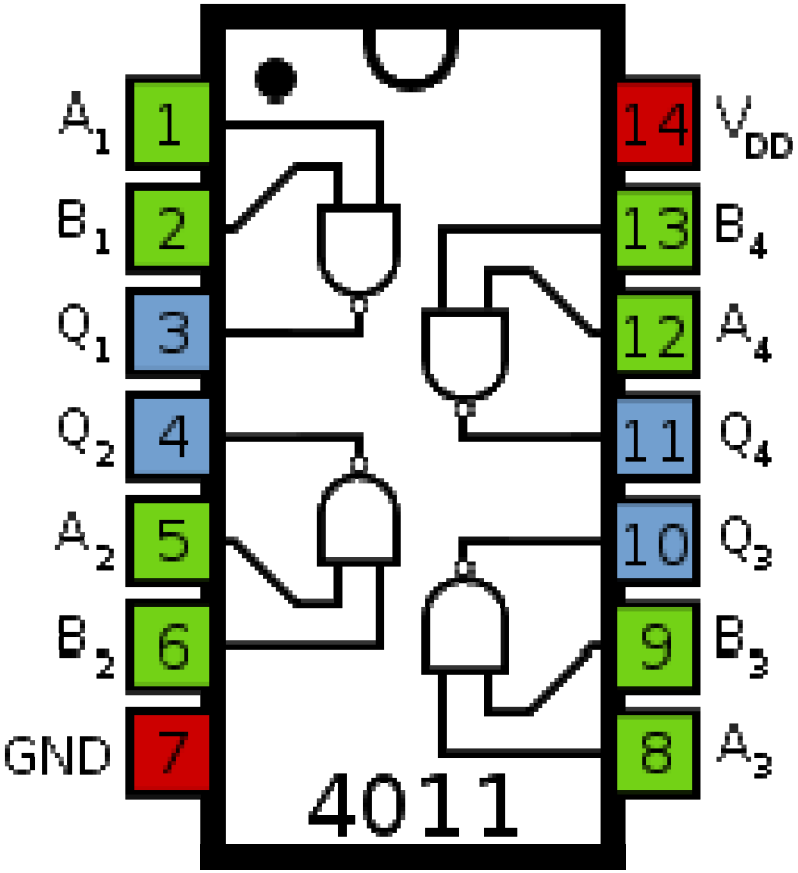

CMOS OR gate
Vdd
Q1
Q2
Q5
Q6
Output
Q3
Q4
InputA
InputB
NOR gate
Inverter

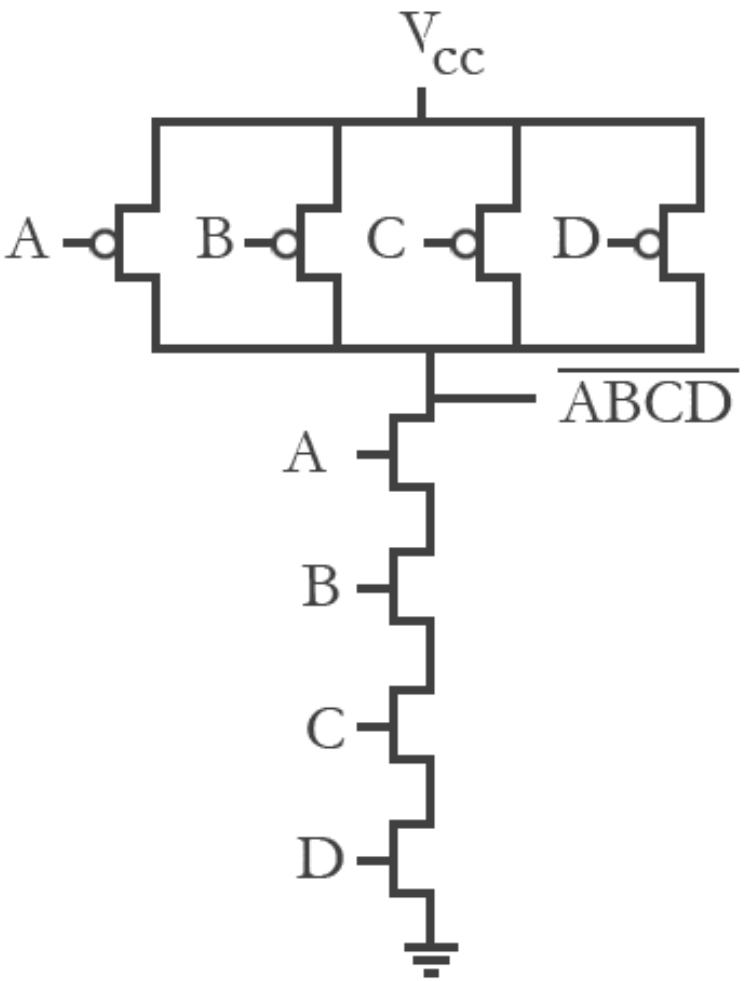

CMOS NOR gate
Vdd
Q1
Q2
Output
Q3
Q4
InputA
InputB

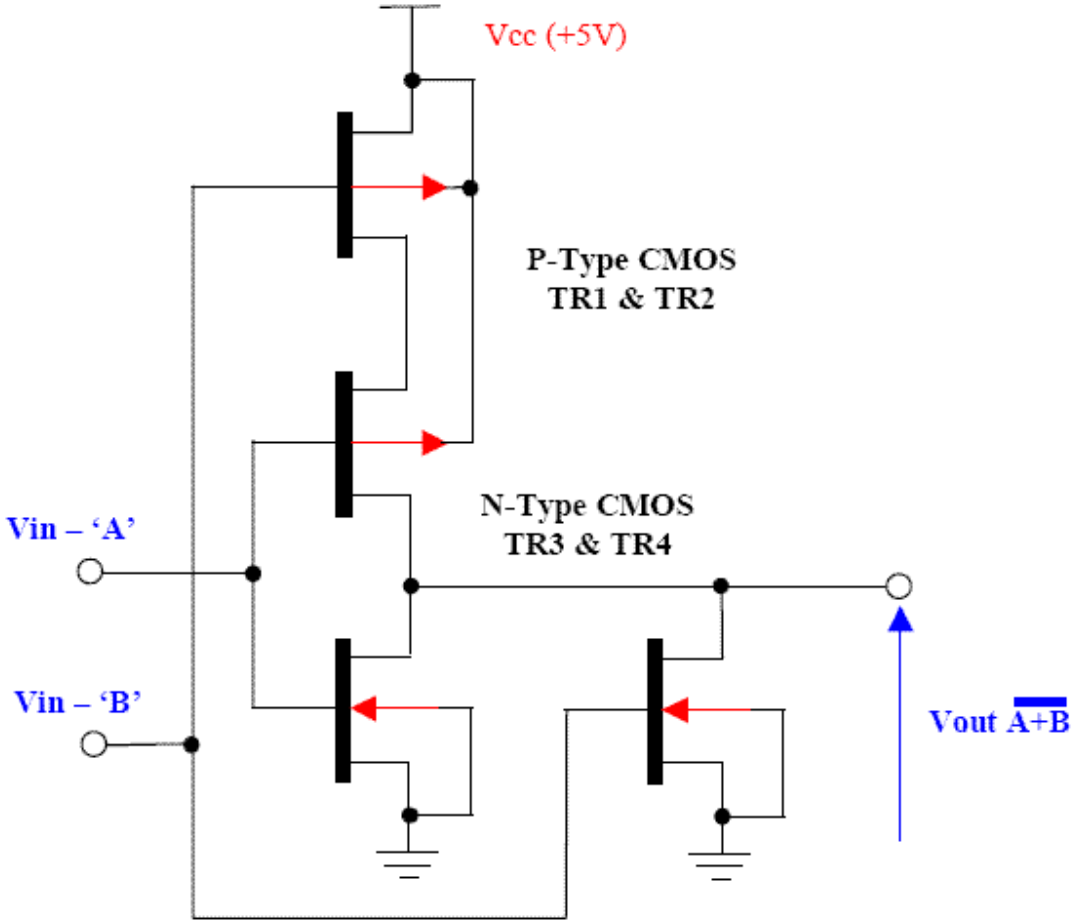

"B-series" (buffered) NOR gate
Vdd
Q1
Q2
Output
Q3
Q4
InputA
InputB

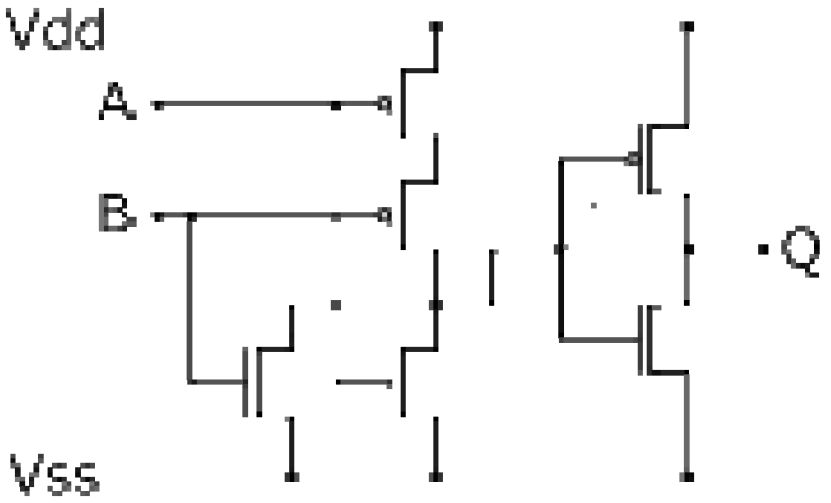
"Pinout," or "connection" diagram for the 4001 quad NOR gate






Vcc
A
B
C
D
ABCD
A
B
C
D

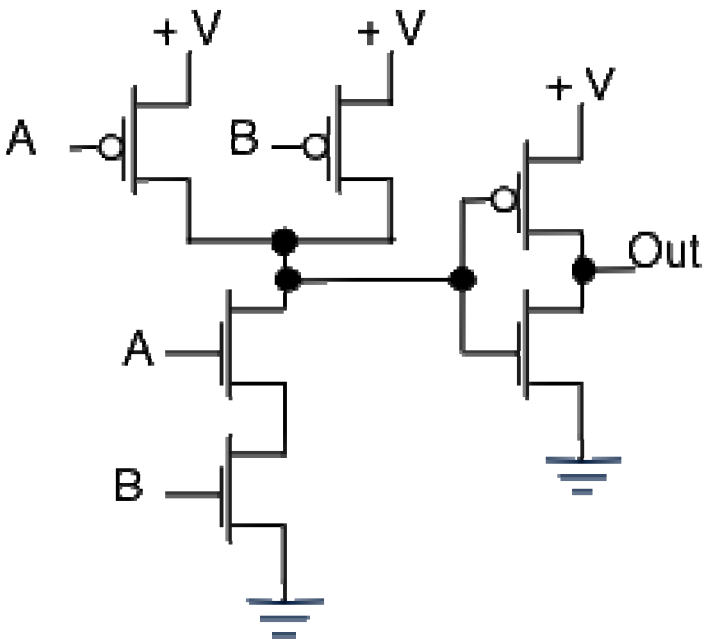

Vcc (+5V)
P-Type CMOS
TR1 & TR2
N-Type CMOS
TR3 & TR4
Vin – 'A'
Vin – 'B'
Vout A+B



OR GATE

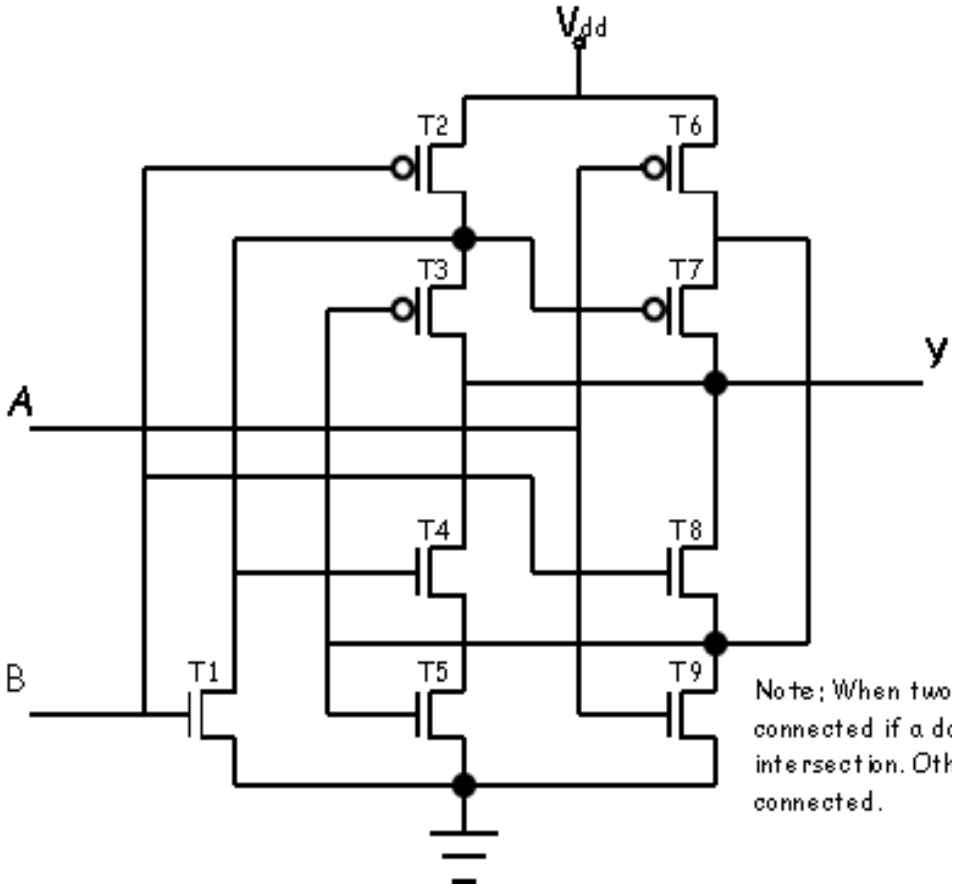
To RELOOK

What are these gates ??



AND GATE

Schematic Diagram



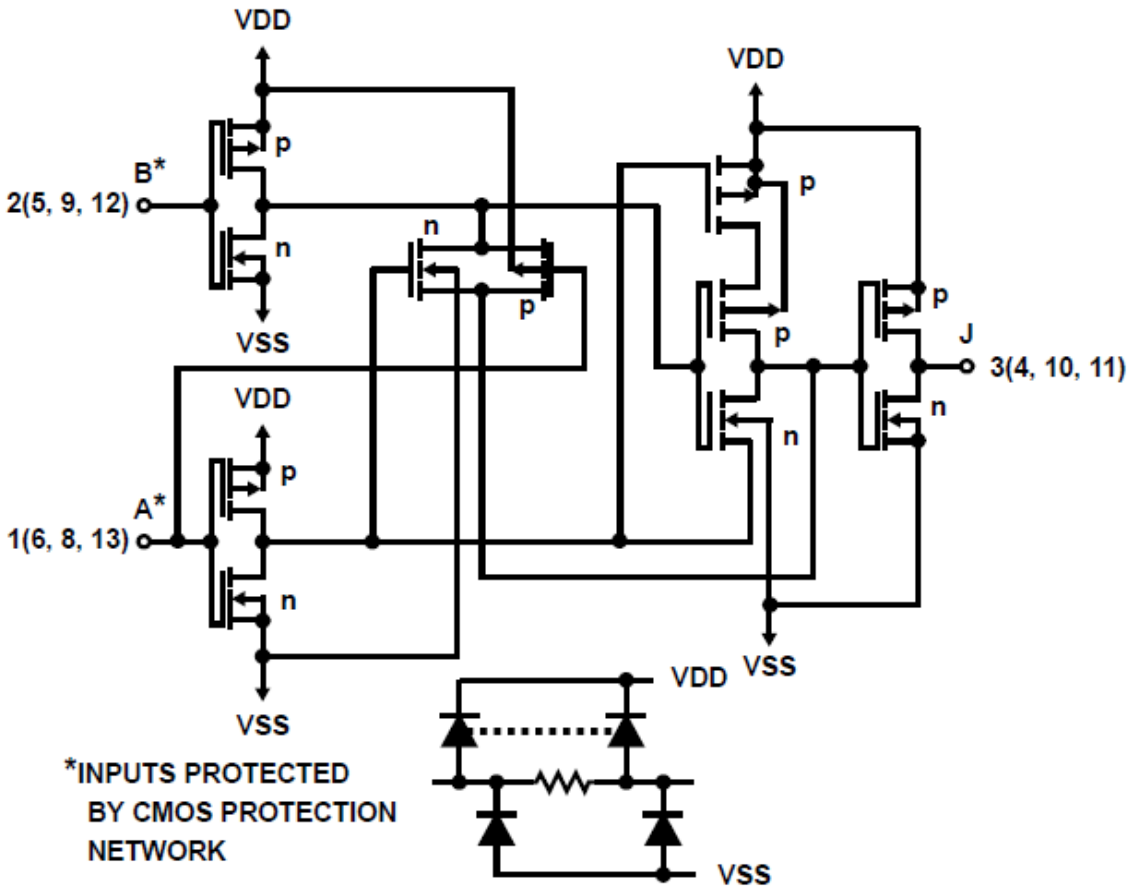
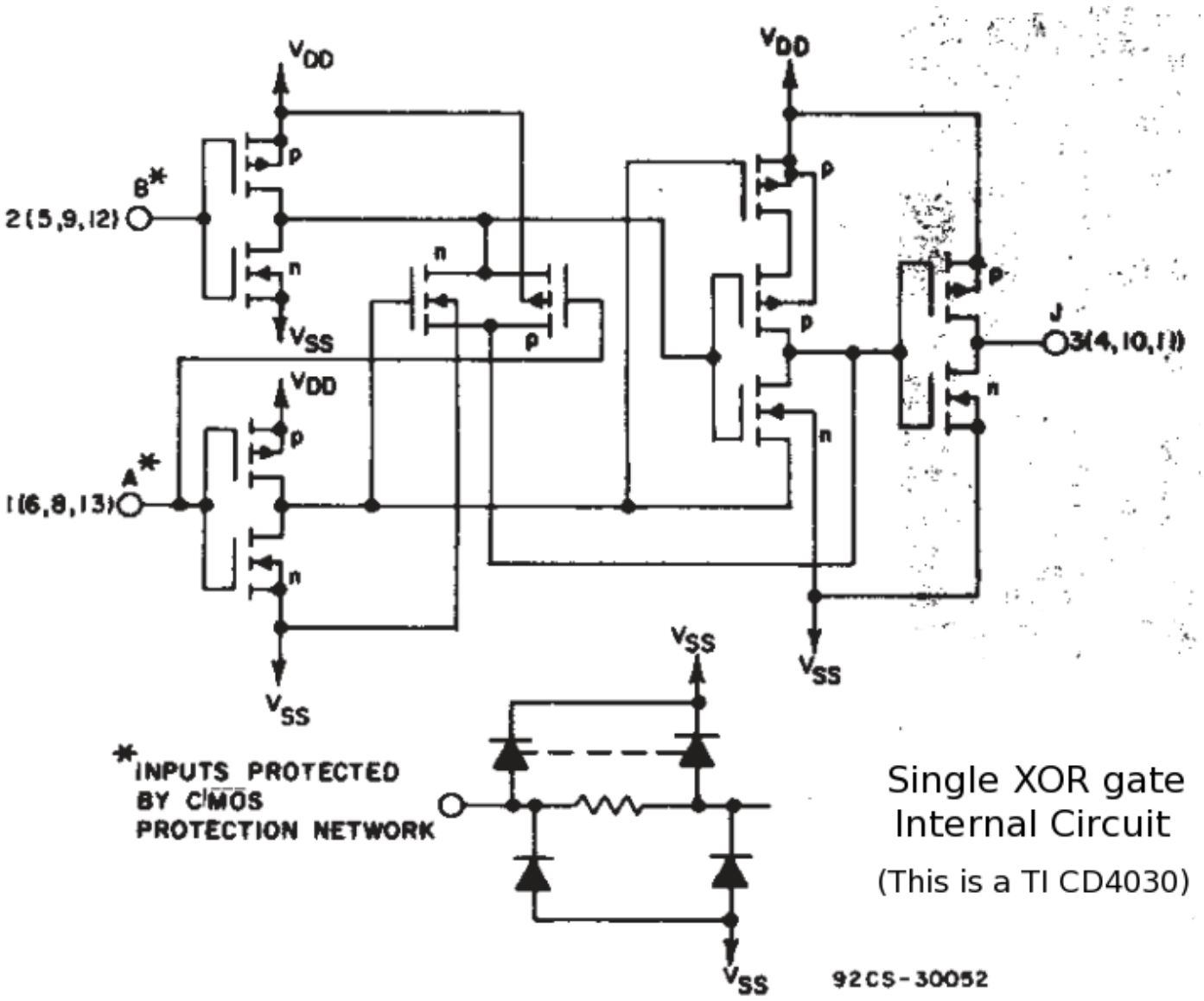
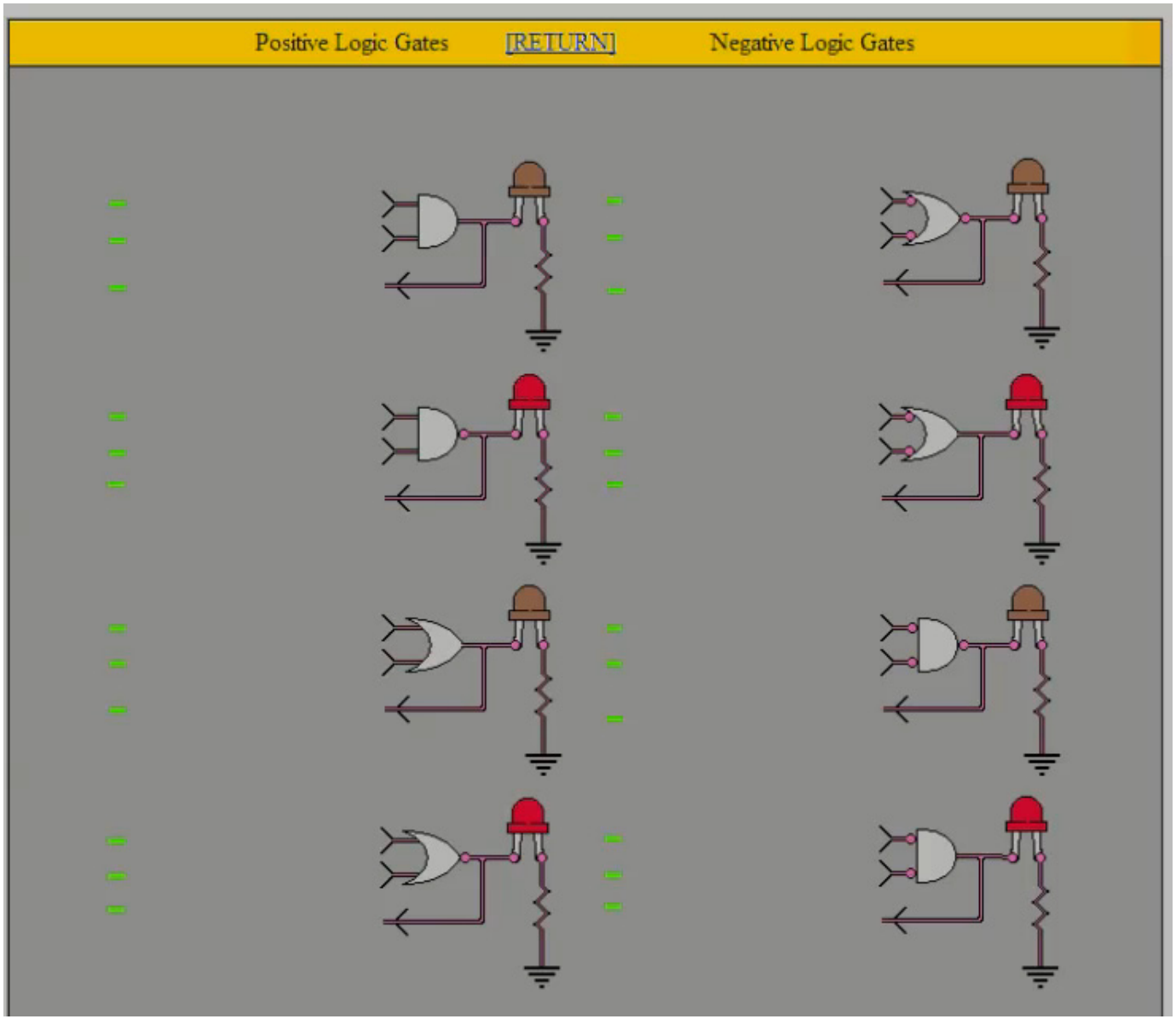


FIGURE 1. 1 OF 4 IDENTICAL GATES



Single XOR gate
Internal Circuit

(This is a TI CD4030)


Positive Logic Gates
[RETURN]
Negative Logic Gates

Dist. Laws:

$X(Y+Z) = XY + XZ;$

$X + YZ = (X+Y)(X+Z);$

$XY + XY' = X;$ $\quad (X + Y)(X + Y') = X;$

$X + XY = X;$ $\quad X(X + Y) = X;$

$(X + Y')Y = XY;$ $\quad XY' + Y = XY;$

De-Morgan's Laws:

$(X + Y)' = X' . Y'$

$(X.Y)' = X' + Y'$

CONSENSUS

$XY + X' Z + YZ = XY + X'Z$

$(X + Y)(X' + Z)(Y+Z) = (X + Y)(X' + Z)$

$F \rightarrow (X + Y')Y = XY$

$F_D \rightarrow XY' + Y = X + Y;$

$F_C \rightarrow X'Y + Y' = X' + Y'$