Digital Logic And Design Laboratory-CS2310

Combinational Circuits

1st Assignment

Introduction to CS2310-Lab, NAND and it's characteristics

2nd Assignment

a.Design Ex-OR

b.Desing Majority gates using NAND and NOR Gates.

3rd Assignment

a.Design a circuit that evaluates the determinant of a 2 X 2 binary matrix (Note : State any assumptions made about input representaion).

b.Design a circuit that takes two unsigned 2-bit numbers (a and b), and displays one of greater(a > b), lesser (a < b) or equal (a == b) signals.

4th Assignment

Half Adder,Full Adder and 4-bit Ripple Carry Adder Implementation.

5th Assignment

Plane Parking problem implementation.

6th Assignment

Cycle Detection in Graphs

7th Assignment

a. Add two 2 digit BCD numbers. Display using 7-segment displays
b. Subtract two 2-digit BCD numbers.

8th Assignment

Convert a 4-bit number for one mode to another. Handle the invalid cases, for both.

a. Gray code to 6-3-1-1 code.
b. Excess-3 code to 2-out-of-5 code.

9th Assignment

Write and Verify Verilog code for 8-bit Multiplier using carry save adders.

Sequential Circuits

10th Assignment

1.) Design two SR Latches, one using NOR gates and another using NAND gates.

2.) Convert the 2 Latches into D Latches.

11th Assignment

Design

a) Master-Slave J-k flip-flop

b) A positive-edge- Triggered T flip-flop using Logic Gates.

12th Assignment

a.) Design a 2-bit Synchronous up counter using D Flip Flop IC's. Display the output on a 7 segment LED display

b.) Counter using asynchronous flipflop arbitrary sequence.

13th Assignment

Sequence generator using shift registers.

Verilog Implementation

14th Assignment

Write and Verify Verilog code for Elevator Design.