CS2310: Digital Logic Design Lab Experiment 4

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Problem Statement

Adders form a core component of the Arithmetic Logic Unit (ALU) and play a major role in calculating memory addresses, table indices etc., in Computer Processors. In this lab, you will be learning and implementing Adder circuits for unsigned numbers.

The *Half adder* takes in two input bits and produces two output bits, the *sum* and the *carry*, the XOR and AND of the two bits respectively.

The *Full adder* takes in two input bits and a third bit (carry-in). It also produces two output bits, the sum and the carry-out. Their truth tables are given below.

Truth table for Half adder

INPUTS		OUTPUTS	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth Table of Full Adder

Inputs			Outputs	
X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Figure 1: Truth tables for Half Adders and Full Adders

A)Half Adders and Full Adders

You will first implement a Half Adder using basic logic gates, and then implement a Full Adder using Half Adders and basic logic gates.

B) Ripple-carry Adders

Connect multiple adders (half/full) to display the 4-bit sum of two 3-bit numbers.