CS2310: Digital Logic Design Lab
Experiment 6

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Problem Statement

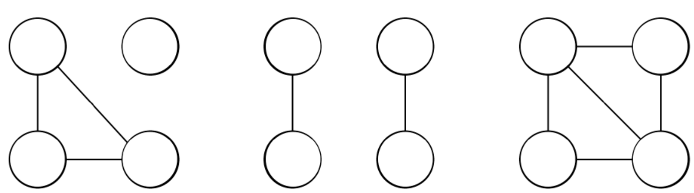
Consider a simple, undirected graph with four vertices. You will design circuits that count the following :-

1. The total number of cycles in the graph.

2. The number of connected components in the graph.

A connected component of an undirected graph is a subgraph in which any two vertices are connected to each other by paths, and which is connected to no additional vertices in the super graph.

For both problems, you will be presenting the output by displaying the corresponding number on a 7-segment display.
You are allowed to use any of the basic logic gates, adders, muxes, decoders and encoders for this assignment.
Hint : Reduce and reuse



(a) One cycle and two connected components

(b) Zero cycles and two connected components

(c) Three cycles and one connected component

Figure 1: Sample undirected graphs with four vertices