

On Saving Energy in Boolean Circuits via Negations

Jayalal Sarma¹ Kei Uchizawa²

¹Indian Institute of Technology Madras, Chennai, India

²Graduate School of Science and Engineering, Yamagata University, Japan

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Energy Complexity in Circuits

Energy of Circuits and Functions

- C be a Boolean circuit over a basis \mathcal{B} for $f : \{0, 1\}^n \rightarrow \{0, 1\}$.

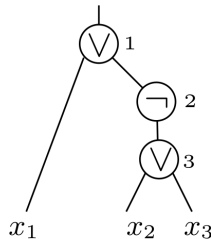
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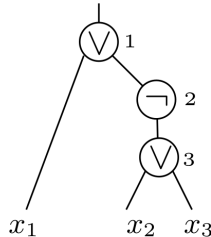
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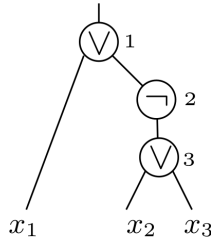
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For $n \in \mathbb{N}$, $EC_{\mathcal{B}}(n) = \max_f EC_{\mathcal{B}}(f)$ where the max is over all n -bit functions.

History of Energy Complexity

Vaintsvaig (1961)

For any finite basis \mathcal{B} , for every $n \in \mathbb{N}$, $\Omega(n) \leq \text{EC}_{\mathcal{B}}(n) \leq O(2^n/n)$

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- $EC(f) \leq DT(f)^3$ (Dinesh *et al* 2020).
- $\sqrt{DT(f)} \leq EC(f) \leq DT(f)^2$ (Sun *et al* 2022)

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A "close variant" - Dichotomy Theorem - Kasim-zade (1992)

Fix a finite basis \mathcal{B} (with d -ary gates for constant d), one of the following must hold:

- For every n , $\Omega(n) \leq \widetilde{\text{EC}}_{\mathcal{B}}(n) \leq O(n^2)$.
- For every n , $2^{n/2d} \leq \widetilde{\text{EC}}_{\mathcal{B}}(n) \leq 2^n/n$.

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$\widetilde{\text{EC}}_{\mathcal{B}}(n)$ counts the gates where the output is 1 or at least one input is 1.

It was also shown that such a dichotomy does not hold for energy complexity $\text{EC}_{\mathcal{B}}(n)$.

Known Results on Specific Basis

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Threshold Basis - \mathcal{B}_{th} with linear threshold functions - (Uchizawa *et al*)

There exists explicit Boolean functions $f : \{0, 1\}^n \rightarrow \{0, 1\}$ such that

- computable by constant-depth and linear-size threshold circuits.
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Bounds parameterized by Fanin - Suzuki *et al* (2013)

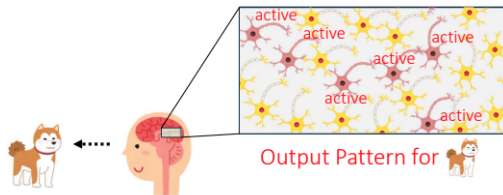
\mathcal{B}_ℓ consisting of arbitrary Boolean functions of fanin ℓ showed that

$$\Omega\left(\frac{n - m_f}{\ell}\right) \leq \text{EC}_{\mathcal{B}_\ell}(f) \leq O\left(\frac{n}{\ell}\right)$$

for any symmetric function f , where m_f is the maximum number of consecutive 0s or 1s in the value vector of f .

Another Motivation for Threshold Basis

- Modeling neural networks as threshold circuits.
- A neuron firing uses energy.
- The brain needs to construct energy efficient output patterns.



Question: *Can we evaluate computational power of a neural network with few number of active neurons?* This leads to energy complexity.

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- More recently, we had shown (2024) that for the standard basis $\mathcal{B}_* = \{\wedge, \vee, \neg\}$ where \wedge and \vee are of unbounded-fanin.

$$\left\{ \begin{array}{l} f \text{ can be computed by a circuit } C \\ \text{of size } s \text{ and energy } e \end{array} \right\} \implies \left\{ \begin{array}{l} \text{Number of output patterns} \\ \text{is at most } 2^{e \log e} \end{array} \right\}$$

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This was further used in to establish lower bounds for the energy over the basis \mathcal{B}_* .

Role of Negations in Saving Energy : The \mathcal{N}_* -basis

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Our Basis - \mathcal{N}_*

Conjunction and disjunction with unbounded fan-in, where any input variable can be negated.

Our Results

Our Results 1: Power of \mathcal{N}_* -Circuits

Universality

For any Boolean function $f : \{0, 1\}^n \rightarrow \{0, 1\}$, there exists an \mathcal{N}_* -circuit of size $|f^{-1}(0)|$ and energy one. $\text{EC}_{\mathcal{N}_*}(n) = 1$.

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Contrast: \mathcal{B}_* -circuits require:

- Energy $\Omega(\sqrt{n})$ to compute PAR_n (defined as $\bigoplus_{i \in [n]}$).
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Number of Output Patterns

There exists a DeMorgan circuit over the basis \mathcal{N}_* of size n , energy e , and $(n/e + 1)^e$ output patterns.

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Contrast : Any \mathcal{B}_* -circuit of energy e has at most $2^{O(e \log e)}$ output patterns.

Our Results 2: From Decision Trees to \mathcal{N}_* -Circuits

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Rank Bound to Energy Bound

If a Boolean function f is computable by a decision tree of size s and rank r , then f is also computable by a \mathcal{N}_* -circuit of size $O(s)$ and energy $O(r)$.

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Contrast: There is a Boolean function that can be computed by a rank 1 Decision tree but every \mathcal{B}_* circuit computing it requires $\Omega(\log n)$ energy.

Our Results 3: Lower Bounds in terms of Size and Depth

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Lower Bounds for DeMorgan Circuits

Let C be a DeMorgan \mathcal{N}_* -circuit computing $\text{PAR}_{[n]}$. Then

$$\text{EC}_{\mathcal{N}_*}(C) \geq \frac{n}{d \log s}$$

where s and d are the size and depth of C , respectively.

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Lower Bounds for Layered Circuits

Let C be a \mathcal{N}_* -circuit of size s and depth d that computes $\text{PAR}_{[n]}$. If every input variable is connected to a gate in the bottom layer, then for sufficiently large n :

$$\text{EC}_{\mathcal{N}_*}(C) \geq \frac{n}{d \log s}$$

Our Results 4: Lower Bounds in terms of Matrix Rank

Let $f : \{0, 1\}^n \times \{0, 1\}^n \rightarrow \{0, 1\}$ be a Boolean function. The communication matrix M_f is a $2^n \times 2^n$ matrix with entry $M_f(x, y) = f(x, y)$.

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Lower Bounds from Rank of the Communication Matrix

If a circuit C on $2n$ vars computes a Boolean function $f : \{0, 1\}^n \times \{0, 1\}^n \rightarrow \{0, 1\}$, and has size s , depth d , then

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- Any \mathcal{N}_* -circuit C is a polynomial-size and constant-depth circuit computing DISJ_n , then C must have energy at least $\Omega(n/\log n)$.
- This is tight! - DISJ_n can indeed be computed by a \mathcal{N}_* -circuit of size $O(n^2/\log n)$, depth 3 and energy $O(n/\log n)$.

A Couple of Proof Ideas

A Distinction between \mathcal{N}_* -circuit and \mathcal{B}_* -circuit

Simplifying \mathcal{B}_* -circuit of small energy

If a Boolean function f is computable by a \mathcal{B}_* -circuit of energy e , then we can force f to be constant by fixing at most $e^2 + e$ variables.

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Corollaries

- Energy $\Omega(\sqrt{n})$ required to compute PAR_n (defined as $\bigoplus_{i \in [n]}$).
- Energy $\Omega(\sqrt{\log n})$ required for computing MUX_n .

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- Write $\neg f$ in the sum of products form and attach a negation to get back f .
- Replace the root \vee gate with negated \wedge gate from \mathcal{N}_* .
- For $a \in \{0, 1\}^n$, if $f(a) = 0$, exactly one of the \wedge gates outputs 1 if $f(a) = 0$.
- For $a \in \{0, 1\}^n$, if $f(a) = 1$, only the root gate outputs 1.
- The size is $|f^{-1}(0)|$ and energy is 1.

From Rank-bounded Decision Trees to \mathcal{N}_* -circuits

Decision tree T of rank r . S_T : the "addresses" of the nodes of the tree.
 L_T : the addresses of the leaves of the tree.

Uchizawa *et al* (2008)

$$\left\{ \begin{array}{l} \text{Decision tree } T \text{ of} \\ \text{size } s \text{ and rank } r \end{array} \right\} \longrightarrow \left\{ \begin{array}{l} \text{Equivalent DT } T' \text{ of size } s \\ \text{such that } \forall a \in L_T, wt(a) \leq r \end{array} \right\}$$

- For each $s \in S_{T'}$, we make a \wedge -gate g_s with fan-in $|s| + 1$, receives the outputs of g_t for each $t \prec s$ (negated if $t0$ is a prefix of s) and the variable x_s .
- Output gate g receives the output of every gate g_t for t satisfying that either

$$“t0 \in L_{T'} \text{ and } \ell_{t0} = 1” \text{ or } “t1 \in L_{T'} \text{ and } \ell_{t1} = 1”$$

and the output is negated for the former case.

- This circuit has size $O(s)$ and energy $r + 1$.

Lower bounds for DeMorgan Circuits over \mathcal{N}_*

Theorem

Let C be a DeMorgan \mathcal{N}_* -circuit computing $\text{PAR}_{[n]}$. Then $\text{EC}_{\mathcal{N}_*}(C) \geq n/(d \log s)$ where s and d are the size and depth of C , respectively.

Aim : To show an input assignment $a \in \{0,1\}^n$ such that at least $n/(d \log s)$ gates output 1.

- Construction is iterative : While $d \log s \leq |I|$, we repeatedly apply a procedure to find a partial assignment of the desired a , and obtain a circuit C' computing $\text{PAR}_{I'}$ for some $I' \subseteq I$ towards the next step.
- In a stage, we will set at most $d \log s$ variables.
- If an \vee gate directly receives an input literal, set the bit and proceed to next stage.

Proof Idea (Contd.)

- No \vee gate receives a direct input literal. Bottom layer is only \wedge gates.
- We will show that there exists an \wedge gate in the bottom layer with fanin at most $d \log s$. We will set the variables and proceed to the next stage.
- We can assume that the circuit has alternating \vee and \wedge gates.
- Suppose for contradiction that every \wedge gate in the bottom layer has fanin larger than $d \log s$.
- Since the circuit is computing parity on $|I|$ variables, we have for each g in the bottom layer:

$$S_1^C(g) \leq 2^{|I| - d \log s} = \frac{2^{|I|}}{s^d}$$

where S_1 is the number of input settings to the circuit which makes g output 1.

Proof Idea (Contd.)

- By an induction on the layers, for each $g \in G_\ell$,

$$S_1^C(g) \leq \frac{2^{|I|}}{s^{d-\ell+1}}$$

- This is a contradiction since the number of assignments that makes the root output 1 will be at most $\frac{2^{|I|}}{s} < 2^{|I|-1}$.
- Hence there must exist an \wedge gate in the bottom layer with fanin at most $d \log s$.
- We set those $d \log s$ bits such that \wedge gate outputs 1 and continue to the next stage.
- Repeat the stages until $d \log s > |I|$.
- Since we are setting the gates to value 1. we should be able to do this only for e steps before hitting the constraint $d \log s > |I|$.
- Hence $n \leq ed \log s$.

A Connection to Rank of the Communication Matrix

- Let C be a \mathcal{N}_* -circuit. For every gate g in C :
 - $I(g)$: input variables that are connected to g
 - $I'(g)$: set of the gates in G_C that feed into g .
- G_C : functions obtained from g by fixing the outputs of the gates in $I'(g)$.
- Define

$$r_C = \max_{g_1, \dots, g_e \in G_C} rk(M)_{\wedge [g_1, \dots, g_e]}$$

Lemma - (Implicit in Uchizawa and Abe (2023))

Let C be a circuit of size s , depth d and energy e . Then it holds that

$$rk(M_C) \leq (s^e \cdot r_C)^{O(d)}.$$

A Connection to Rank of the Communication Matrix

Observe that our functions in G_C can be only \wedge , \vee and constant functions. We show $r_C \leq 2^e$ and this derives our result.

Theorem

If a \mathcal{N}_* -circuit C computes a Boolean function of $2n$ variables, has size s , depth d and energy e , then it holds that

$$\log(\text{rk}(M_C)) = O(ed \log s)$$

Other Applications

- Let $f : \{0, 1\}^n \rightarrow \{0, 1\}$ be a Boolean function. Let $g : \{0, 1\}^2 \rightarrow \{0, 1\}$ be a 2-bit gadget function. Define $F_g : \{0, 1\}^n \times \{0, 1\}^n \rightarrow \{0, 1\}$ defined as $F_g(x, y) = f(z_1, z_2, \dots, z_n)$ where $z_i = g(x_i, y_i)$.
- Let M_f^g for the matrix M_{F_g} .
- Let M_f^* be a matrix that satisfies

$$rk(M_f^*) = \max(rk(M_f^\wedge), rk(M_f^\vee))$$

- Shrestov (2010): for any Boolean function f , the $\deg(f)$ is upper bounded by $rk(M_f^*)$.

Corollary

If a circuit C of size s , depth d , computes a Boolean function F such that $M_F = M_f^*$, then it holds that $\text{EC}_{\mathcal{N}_*}(C) \geq \Omega\left(\frac{\deg(f)}{d \log s}\right)$

Conclusion and Open Problems

Conclusion and Open Problems

- We showed upper and lower bounds for Energy complexity over the \mathcal{N}_* .
- Motivation is to understand the power and limitations of negations in saving energy.
- Shortcoming: ideally we would like to have design techniques where negations can be used to switch off "irrelevant parts" of the circuit.
- Can we relate the energy over \mathcal{N}_* to other Boolean complexity measures?
- Lower bound techniques for energy complexity? Limitations?

Thank you for your attention.

Questions?