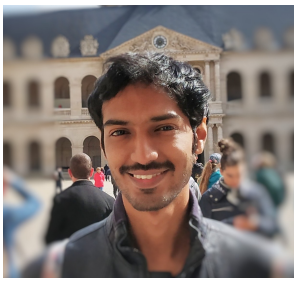

Prasanna Karthik Vairam

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Education and Work Experience

2014 – 2020 (Jan)	**Doctor of Philosophy (Ph.D.)**
	IIT Madras, Chennai, India. Grade: 9.25/10
	Advisors: Prof. Chester Rebeiro & Prof. Kamakoti V
2011 – 2014	**Work Experience**
	Intel Technology India Pvt. Ltd, Bangalore, India.
	Position: Graphics Hardware Engineer
2009 – 2011	**Master of Technology (M.Tech)**
	IIT Bombay, Maharashtra, India. Grade: 8.94/10
	Advisor: Prof. Kameswari Chebrolu
2005 – 2009	**Bachelor of Engineering (B.E)**
	Anna University, Chennai, India. Grade: 83.8/100
2003 – 2005	**Senior High school (Class XII)**
	PSBB Schools, Chennai, India. Grade: 85/100
1994 – 2003	**High School (Class X)**
	Kendriya Vidyalaya, Chennai, India. Grade: 87.4/100

Honors and Awards

- Awarded the highly competitive *Institute Research Award* by IIT Madras for quality and quantity of research publications.
- Won the 1st place in the Embedded Security Challenge conducted as a part of Cyber Security Awareness Week (CSAW'16) by New York University.
- Won the 1st place in the Applied Research Competition conducted as a part of Cyber Security Awareness Week (CSAW'18) by New York University.
- Won 2nd place in the Doctoral Colloquium conducted by IDRBT (Research wing of Reserve Bank of India).
- Secured the 117^{th} rank among 50,000 candidates who wrote the National graduate entrance exam (GATE) in India.
- Awarded grants for travelling to top ranking conferences by Microsoft Research India and Kris Gopalakrishnan Endowment.
- Awarded the *Gandhi Hazare Award* for using technology to fight corruption in India.
- Awarded the *AWSAR Science Story Writing Award* for one of the top 100 stories (Rank: 20) in India across all scientific fields, conducted by Department of Science and Technology, Government of India.
- Awarded the *Star Teaching Assistant* prize by the Department of Computer Science and Engineering, IIT Madras.

Areas of Interest & Technical Skill Set (Past inclusive)

Areas of Interest: Computer Networks, Computer Architecture, and VLSI Design.
Programming/Scripting Languages: C,C++, Python, PHP, Shell
Operating Systems: Linux, Windows, Embedded Linux
Databases: MySQL
Tools: Beamer, LaTeX
Network Simulators: NS2, NS3, Qualnet, Mininet
Device Drivers/OS: Intel DPDK suite (x86), Madwifi-Linux(802.11), Tiny OS(802.15.4)
HDL: Verilog, VHDL, Bluespec

Ph.D. Dissertation [Aug. 2014 – Present]

Applications of Approximate data structures in Resource-Constrained Networks

*(**PhD Dissertation**, July 2014 - Jan 2020 (Expected), Guided by Prof. Kamakoti and Prof. Chester)*

- Approximate data structures require less storage and computation but result in slight loss of accuracy. However, the applicability of such data structures in an untrusted environment is still a challenge today. As a part of this thesis, we show how we can design, implement, and use approximate data structures for solving critical problems in a resource-constrained networks where the network nodes are untrusted.
- The first problem that we studied is the measurement of quality of service (QoS) of a service element (e.g., webserver, firewall) in a service function chain (SFC). Most existing solutions for this problem assume that a majority of the service elements are trusted. Solutions for untrusted environments incur unreasonable storage and communication overheads. We propose a novel scheme, based on the evidence Bloom filter (e-BF) for measuring QoS reliably. Our solution can provide highly accurate QoS measurements with 97% accuracy even in adversarial conditions, while the storage and communication overheads are minimal.
- In the second problem, we extend the applicability of Blockchains to resource constrained settings such as Internet of Things (IoT). The Blockchain technology is known to provide verifiable tamper-resistant trails of accepted transactions. However, this comes at the considerable cost of storage and computational power, thereby restricting its application in resource constrained settings. Current research has focused on alternatives such as proof-of-reputation and proof-of-stake to reduce the burden on the participants. Orthogonal to this effort, we focus on the applicability of Blockchains to a specific set of applications that do not require a 100% tamper resistant transaction trail. To this end, we introduce two Blockchain design alternatives which are based on hash tables and e-BF.
- In the third problem, we extend the applicability of Physically Unclonable Functions (PUF) to a resource-constrained P2P network. PUF is a popular hardware technology that uses the naturally occurring variations in microprocessors to distinguish between embedded devices. The storage and computational overheads of traditional PUF-based protocols are significant, thereby making it unsuitable for resource-constrained embedded devices. In this work, we propose TinyPUF, a light-weight PUF protocol that incurs low overheads at both the prover and the verifier. TinyPUF uses novel techniques to compress and store the Challenge-Response pairs (CRPs) at the verifier. We show that the techniques used to compress are carefully designed such that they have little or no impact on the accuracy of authentications. The proposed technique is able to reduce the storage overheads at the verifier by 75%.
- In the fourth problem, we solve a fundamental long-standing problem of Bloom filters when operating on a stream of data: as a Bloom Filter fills up over time, the False Positive rate increases. The critical insight behind our solution is based on the DRAM technology: If the periodic refresh of DRAM cells are disabled, then a data element that is not accessed frequently will predictably lose charge and be naturally flushed. With data derived from a real networking application, we show that for standard DRAM retention rates, our variant significantly improves upon the False Negative and False Positive guarantees of traditional Bloom Filter variants. We believe that our solution offers a practical solution for embedded networking systems with tight design constraints.

Work Experience at Intel Technology India Pvt. Ltd. [Aug. 2011 – Jun. 2014]

- Worked on building the C++ based reference model of Intel's HD Graphics solutions for 3 projects. The nature of work involved building the reference model based on the behavioral specification, and developing the validation plan for testing the hardware against the reference model.
- Worked on VS(Vertex Shader), Graphics Performance Monitor, Workload Submission and Input Assembler Units of the 3D Graphics pipeline over a period of 2 years and 11 Months.
- Worked as a part of the team that designed an innovative and scalable methodology for developing test content for 3D Graphics pipeline.
- Conceived idea for validating hardware features that span multiple clusters using machine learning techniques. This work is currently transitioning from concept to development.
- Developed Real-World Usage based Pre-Silicon test content for context switching scenarios between 3D and GPGPU workloads.
- References: Tarun Belagodu (Intel Folsom), Hema Nalluri (Intel Bangalore) and Hariharan S (Intel Bangalore).

Masters Dissertation and Research Projects [Aug. 2009 – Jun. 2011]

Performance enhancement of Wireless Mesh Networks using Dual Radios

*(**MTech Thesis**, Autumn 2010 - Spring 2011, Guided by Prof. Kameswari Chebrolu)*

- This project involves equipping each node of a wireless mesh network with two transceivers and leveraging on the availability of the additional resource to improve the performance of the network.
- Analyzed the feasibility of equipping each node with two transceivers (possibly working on 802.11a/b/g or 802.15.4). This is important as one transceiver may possibly interfere with the working of the other. Based on this study, the IEEE 802.15.4 platform was identified to be the most suitable platform.
- Designed a TDMA based MAC protocol for dual radios that alleviates the SPI bottleneck problem that is present in a TMote-Sky hardware that is based on the IEEE 802.15.4 standard. This protocol was observed to give a throughput enhancement of about 70% over the current state-of-the-art single radio protocol.
- Two Dual radio hardware platforms were also explored, as there is no commercially available dual radio hardware available currently.
- A Dual radio software stack was also written in TinyOS. This radio stack exposes the much necessary API's that are required by the higher level modules to take advantage of the two radios. This dual radio software stack can be reused with any dual radio platform with a few changes.

Simulation of a dynamic TDMA MAC protocol for MANETs

*(**R & D Project**, Autumn 2010, Guided by Prof. Anirudha Sahoo)*

- Designed and simulated a dynamic TDMA protocol for real-time applications, suiting the needs of a war-like environment that are characterized by excessive mobility. The designed protocol could be deployed on sensor motes that act as the soldier's phone. Worked on **500 KLOC** of Qualnet simulator code. This work is supported by **Defence Research & Development Organization (DRDO)**.

Network Management Tools & Techniques: A Survey

*(**MTech Seminar**, Spring 2010, Guided by Prof. Kameswari Chebrolu)*

- This work surveys the existing *state of the art* tools and techniques available to manage networks and compares them on the basis of their applicability, complexity and performance. The report also gives suggestions to network administrators who are on the verge of adopting a tool/technique.

M.Tech. & Ph.D. Course Work

Advanced Computer Networks, Mobile Computing, Network Security, Distributed Systems, Advanced Wireless Networks, Advanced Computer Architecture, Applied Economics and New Trends in IT (Virtualization and Cloud Computing), Digital Systems Testing, Advanced Datastructures and Algorithms, CAD for VLSI Design.

Peer-Reviewed Publications

INFOCOM'19 – Towards Measuring Quality of Service in Untrusted Multi-Vendor Service Function Chains: Balancing Security and Resource Consumption, Prasanna Karthik Vairam, Gargi Mitra, Vignesh Manoharan, Chester Rebeiro, Byrav Ramamurthy, Kamakoti Veezhinathan, IEEE International Conference on Computer Communications, INFOCOM, 2019. [top-tier conference in computer networking, acceptance rate-19%]

ComStd'18 – ApproxBC: Blockchain Design Alternatives for Approximation-Tolerant Resource-Constrained Applications, Prasanna Karthik Vairam, Gargi Mitra, Chester Rebeiro, Byrav Ramamurthy, Kamakoti Veezhinathan IEEE Communications Standards Magazine (ComSTD'18), 2018.

ESL'18 – GANDALF: A fine-grained hardware-software co-design for preventing memory attacks, Gnanambikai Krishnakumar*, Patanjali SLPSK*, Prasanna Karthik Vairam*, Chester Rebeiro, Kamakoti Veezhinathan Embedded Systems Letters (ESL'18), 2018.

ICCAD'19 – Karna: A gate-sizing based Security Aware EDA Flow for Improved Power Side-Channel Attack Protection, Patanjali SLPSK, Prasanna Karthik Vairam, Chester Rebeiro, Kamakoti Veezhinathan, International Conference on Computer Aided Design (ICCAD), 2019 (To appear). [top-tier conference in VLSI design, acceptance rate-23%]

SIGCOMM'19 – White Mirror: Leaking Sensitive Information from Interactive Netflix Movies using Encrypted Traffic Analysis, Gargi Mitra, Prasanna Karthik Vairam, Patanjali SLPSK, Nitin Chandrachoodan, Kamakoti Veezhinathan, ACM SIGCOMM, Poster Paper, 2019. [top-tier conference in computer networking]

COMCOM'20 – Net-Police: A Network Patrolling Service for Effective Mitigation of Volumetric DDoS Attacks, Sareena Karapoola, Prasanna Karthik Vairam, Shankar Raman, Kamakoti V, Elsevier Computer Communications, 2020 (To appear).

Posters

DAC'19 – Karna: A Security Aware EDA Flow for Improved Side-Channel Attack Protection, Patanjali SLPSK, Prasanna Karthik Vairam, Chester Rebeiro, Kamakoti Veezhinathan, Design Automation Conference (DAC) Work-in-progress, 2019. [top-tier conference in VLSI design]

IMC'17 – Samata: A Framework for identifying Net-Neutrality Violations using Evidence Structures, Prasanna Karthik Vairam, Karan Saxena, Gargi Mitra, Chester Rebeiro, Kamakoti Veezhinathan, ACM Internet Measurement Conference (IMC'17), Poster Session, London, United Kingdom, 2017

IMC'17 – Hastakshara: A Passive Side Channel Based Webpage Fingerprinting Attack for Uncovering Client Intent, Gargi Mitra, Prasanna Karthik Vairam, Kamakoti Veezhinathan, Nitin Chandrachoodan, ACM Internet Measurement Conference (IMC'17), Poster Session, London, United Kingdom, 2017.

Professional services

- Program Committee: ACM Mobicom S3 Workshop 2019.
- Reviewer for IEEE Journal on Selected Areas in Communications.
- Reviewer for ACM Transactions on Embedded Computing Systems (TECS).
- Sub-Reviewer: Conference on principles of distributed systems (OPODIS) 2019.
- Shadow PC: ACM Internet Measurement Conference 2018.
- Shadow PC: IFIP Network Traffic Measurement and Analysis 2018.
- Department Consultative Committee's PhD student representative at IIT Madras during 2017-18.