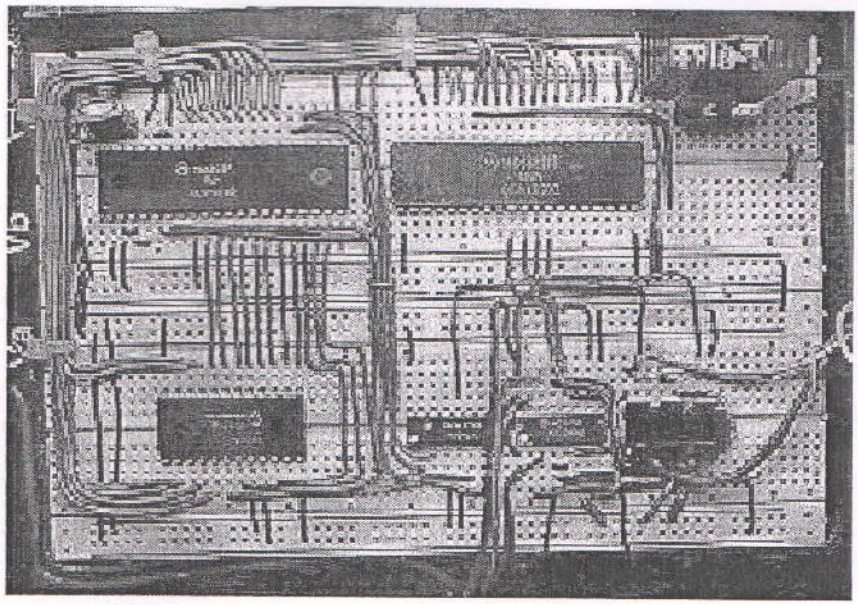


Breadboarding tips:

It is important to breadboard a circuit neatly and systematically, so that one can debug it and get it running easily and quickly. It also helps when someone else needs to understand and inspect the circuit. Here are some tips:

1. Always use the side-lines for power supply connections. Power the chips from the side-lines and not directly from the power supply.

2. Use black wires for ground connections (0V), and red for other power connections.

3. Keep the jumper wires on the board flat, so that the board does not look cluttered.

4. Route jumper wires around the chips and not over the chips. This makes changing the chips when needed easier.

5. You could trim the legs of components like resistors, transistors and LEDs, so that they fit in snugly and do not get pulled out by accident.

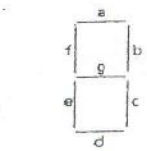
TYPES SN5446A, '47A, '48, '49, SN54L46, 'L47, SN54LS47, 'LS48, 'LS49, SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

scription

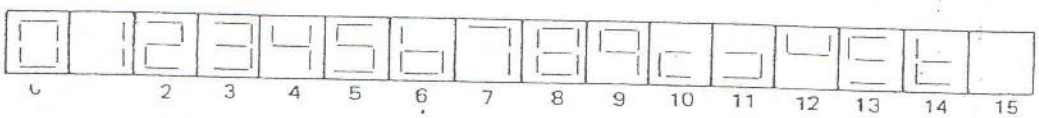
The '46A, 'L46, '47A, 'L47, and 'LS47 feature active-low outputs designed for driving common-anode VLEDs or incandescent indicators directly, and the '48, '49, 'LS48, 'LS49 feature active-high outputs for driving lamp buffers or common-cathode VLEDs. All of the circuits except '49 and 'LS49 have full ripple-blanking input/output controls and a lamp test input. The '49 and 'LS49 circuits incorporate a direct blanking input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

The '46A, '47A, '48, 'L46, 'L47, 'LS47, and 'LS48 circuits incorporate automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is at a high level. All types (including the '49 and 'LS49) contain an overriding blanking input (BI) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs.

The SN54246/SN74246 through '249 and the SN54LS247/SN74LS247 through 'LS249 compose the 6 and the 9 with tails and have been designed to offer the designer a choice between two indicator fonts. The SN54249/SN74249 and SN54LS249/SN74LS249 are 16-pin versions of the 14-pin SN5449 and 'LS49. Included in the '249 circuit and 'LS249 circuits are the full functional capability for lamp test and ripple blanking, which is not available in the '49 or 'LS49 circuit.



SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

'46A, '47A, 'L46, 'L47, 'LS47 FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO[1]	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

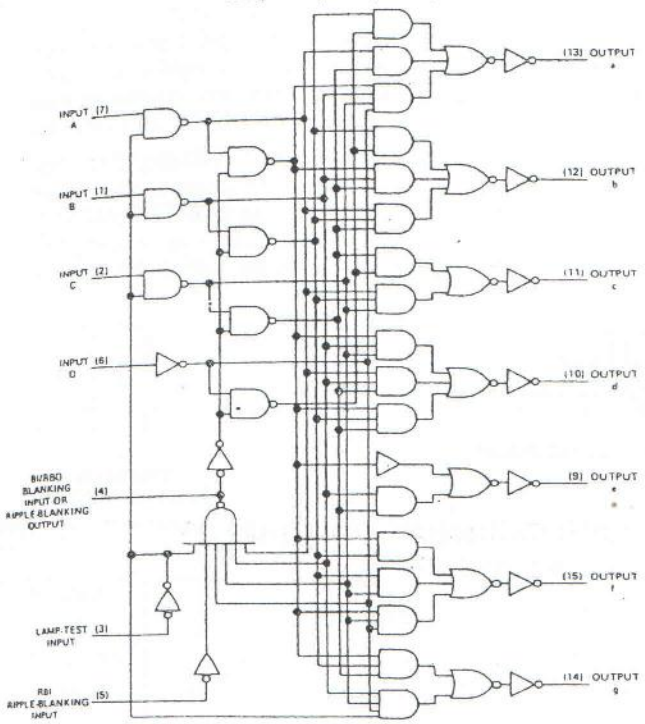
)h level, L = low level, X = irrelevant

1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

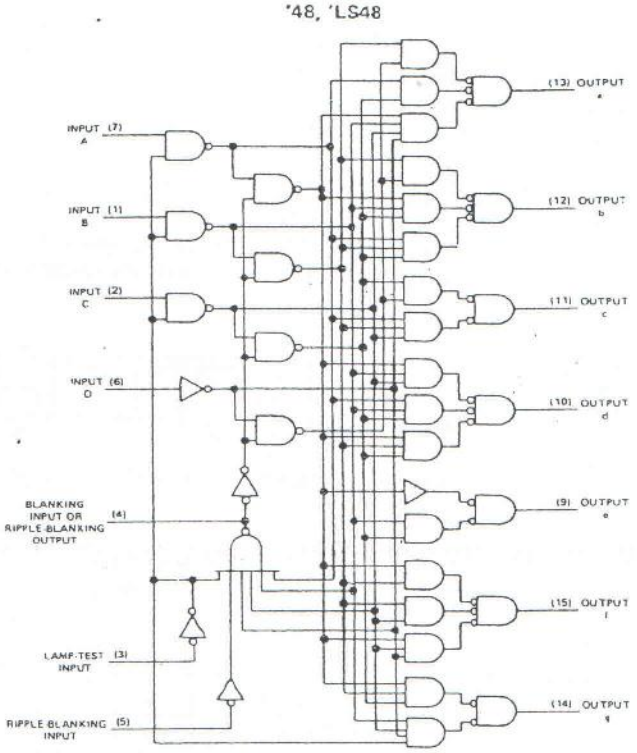
O is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

functional block diagrams

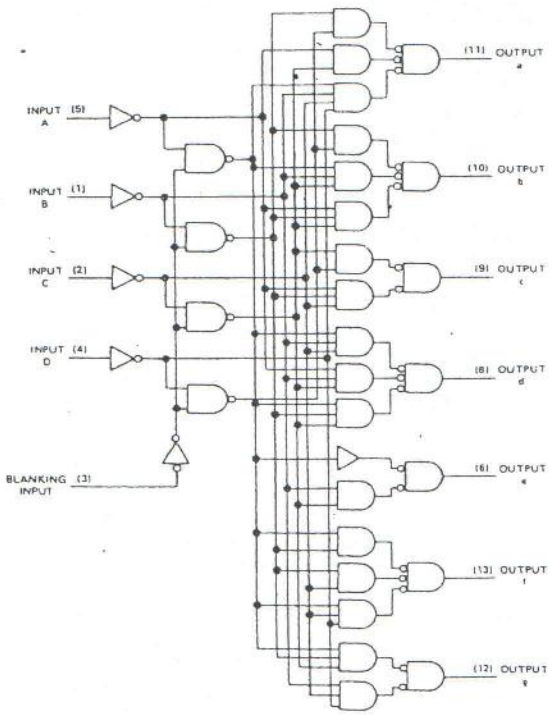
'46A, '47A, 'L46, 'L47, 'LS47



'48, 'LS48



'49, 'LS49



TYPES SN54157, SN54L157, SN54LS157, SN54LS158, SN54S157, SN54S158, SN74157, SN74LS157, SN74LS158, SN74S157, SN74S158
QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7711847, MARCH 1974—REVISED AUGUST 1977

features

- Buffered Inputs and Outputs
- Three Speed/Power Ranges Available

TYPES	TYPICAL AVERAGE PROPAGATION TIME	TYPICAL POWER DISSIPATION
'157	9 ns	150 mW
'L157	18 ns	75 mW
'LS157	9 ns	49 mW
'S157	5 ns	250 mW
'LS158	7 ns	24 mW
'S158	4 ns	195 mW

applications

- Expand Any Data Input Point
- Multiplex Dual Data Buses
- Generate Four Functions of Two Variables (One Variable Is Common)
- Source Programmable Counters

description

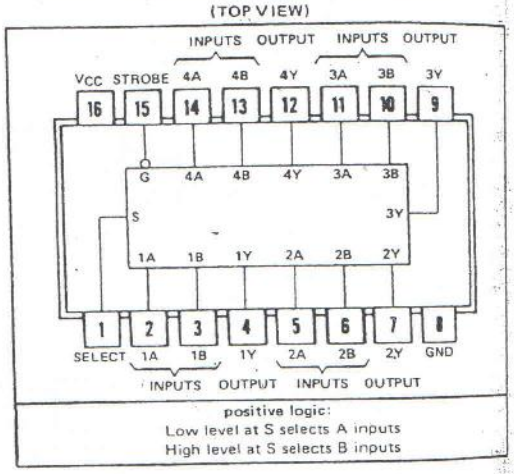
These monolithic data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The '157, 'L157, 'LS157, and 'S157 present true data whereas the 'LS158 and 'S158 present inverted data to minimize propagation delay time.

FUNCTION TABLE

INPUTS				OUTPUT Y	
STROBE	SELECT	A	B	'157, 'L157, 'LS157, 'S157	'LS158 'S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

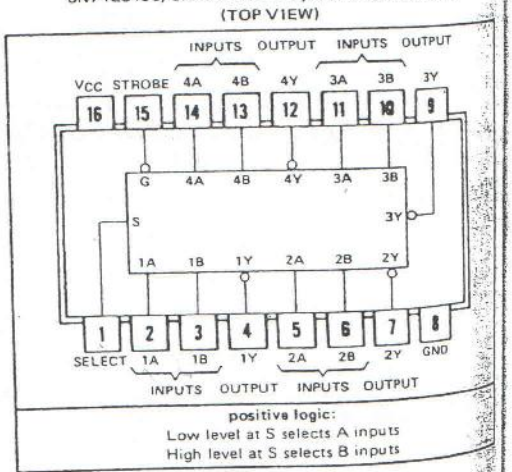
H = high level, L = low level, X = irrelevant

SN54157, SN54LS157, SN54S157 . . . J OR W PACKAGE
SN54L157 . . . J PACKAGE
SN74157 . . . J OR N PACKAGE
SN74LS157, SN74S157 . . . J, N OR NS PACKAGE
(TOP VIEW)



positive logic:
Low level at S selects A inputs
High level at S selects B inputs

SN54LS158, SN54S158 . . . J OR W PACKAGE
SN74LS158, SN74S158 . . . J, N OR NS PACKAGE
(TOP VIEW)



positive logic:
Low level at S selects A inputs
High level at S selects B inputs

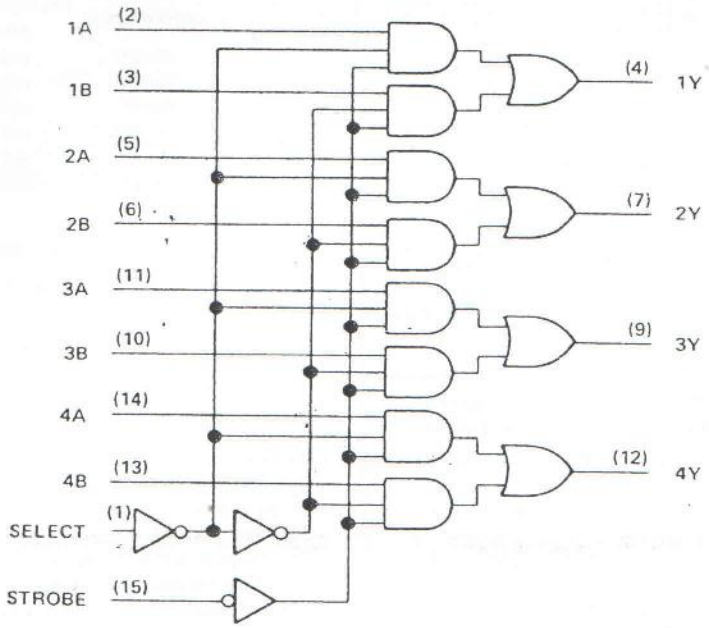
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 5.5 V
Input voltage: '157, 'L157, 'S158 . . . . . 5.5 V
'LS157, 'LS158 . . . . . 7 V
Operating free-air temperature range: SN54', SN54L', SN54LS', SN54S' Circuits . . . . . −55°C to 125°C
SN74', SN74LS', SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

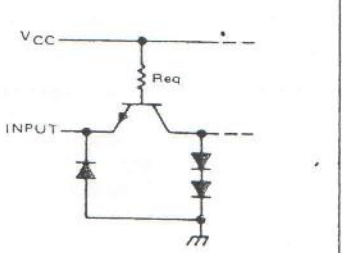
functional block diagram

'157, 'L157



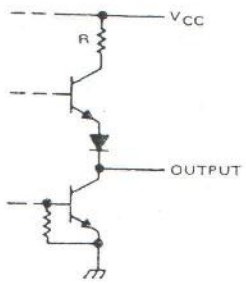
schematics of inputs and outputs

'157, 'L157
EQUIVALENT OF EACH INPUT



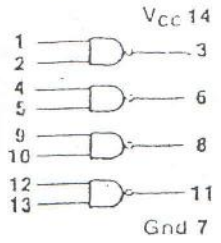
'157: Req = 4 kΩ NOM
'L157: Req = 8 kΩ NOM

'157, 'L157
TYPICAL OF ALL OUTPUTS



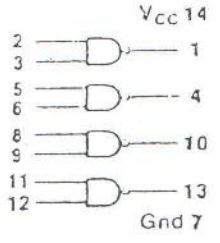
'157: R = 100 Ω NOM
'L157: R = 200 Ω NOM

54/7400 Quad 2-input NAND Gate

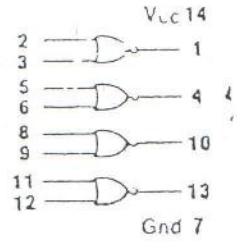


54/7401 Quad 2-input NAND Gate

Free collector outputs

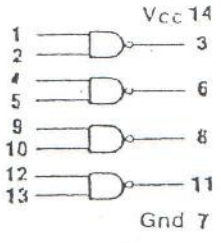


54/7402 Quad 2-input NOR Gate

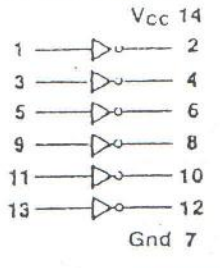


54/7403 Quad 2-input NAND Gate

Free-collector outputs

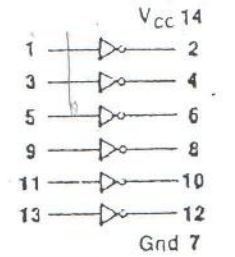


54/7404 Hex Inverter



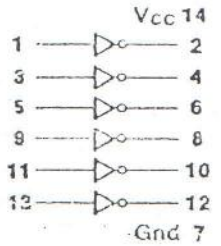
54/7405 Hex Inverter

Free-collector outputs



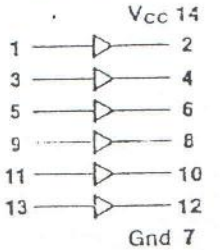
54/7406 Hex Inverting Buffer

Free-collector outputs, 30V rating

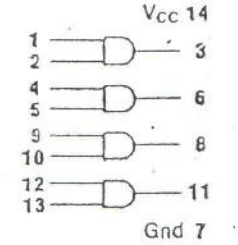


54/7407 Hex Buffer

Free-collector outputs, 30V rating

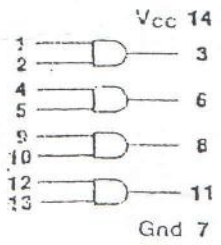


54/7408 Quad 2-input AND Gate

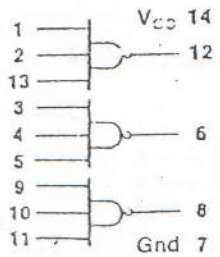


54/7409 Quad 2-input AND Gate

Free-collector outputs

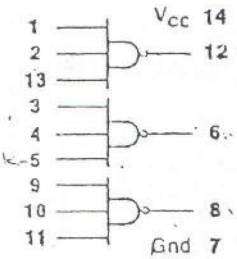


54/7410 Triple 3-input NAND Gate

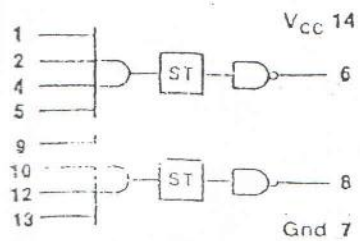


54/7412 Triple 3-input NAND Gate

Free-collector outputs

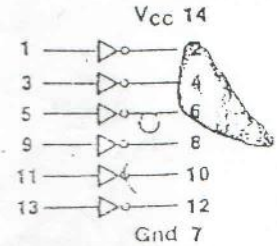


54/7413 Dual NAND Schmitt Trigger



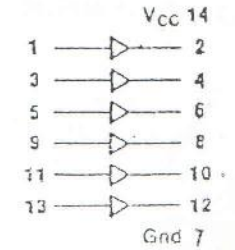
54/7416 Hex Inverting Buffer

Free-collector outputs, 15V rating

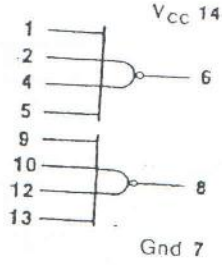


54/7417 Hex Buffer

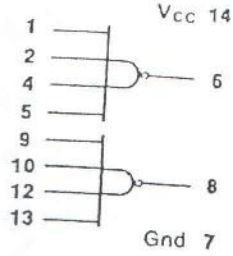
Free-collector outputs, 15V rating



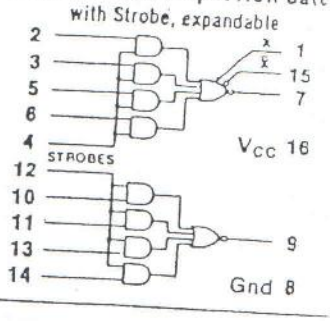
54/7420 Dual 4-input NAND Gate



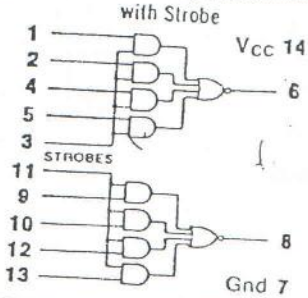
54/7422 Dual 4-input NAND Gate
Free-collector outputs



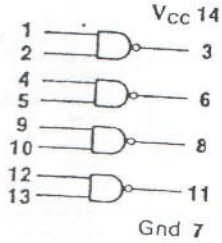
54/7423 Dual 4-input NOR Gate
with Strobe, expandable



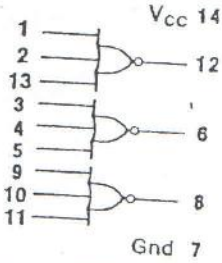
54/7425 Dual 4-input NOR Gate
with Strobe



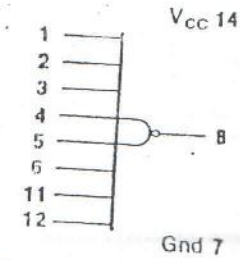
54/7426 Quad 2-input NAND Gate
Free-collector outputs, 15V rating



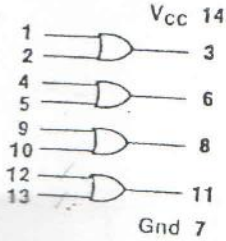
54/7427 Triple 3-input NOR Gate



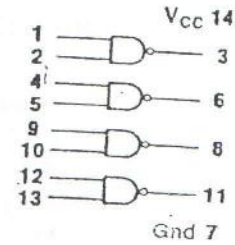
54/7430 8-input NAND Gate



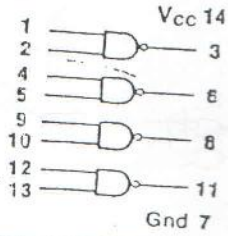
54/7432 Quad 2-input OR Gate



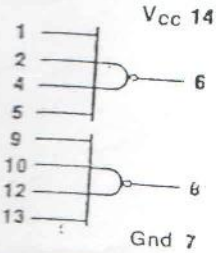
54/7437 Quad 2-input NAND Buffer



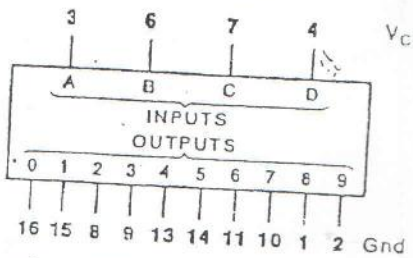
54/7438 Quad 2-input NAND Buffer
Free-collector outputs



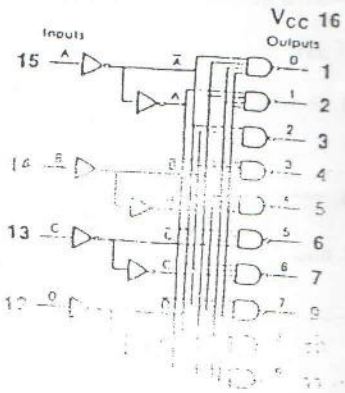
54/7440 Dual 4-input NAND Buffer



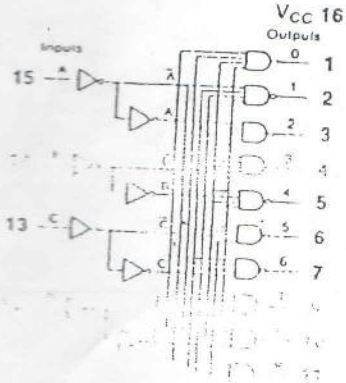
7441A BCD-to-Decimal Decoder/Driver



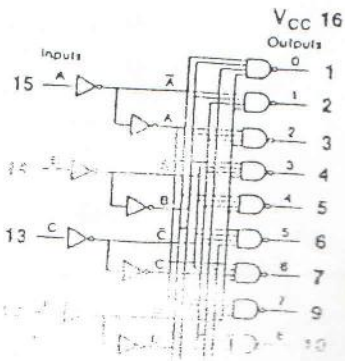
54/7442 BCD-to-Decimal Decoder



54/7443 EXCESS-3-to-Decimal Decoder

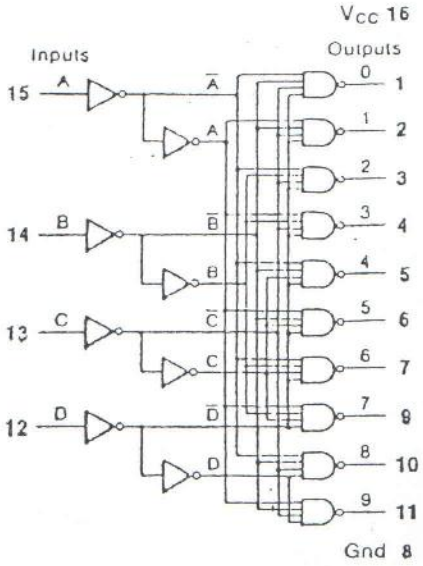


54/7444 EXCESS-3 GRAY-to-Decimal Decode



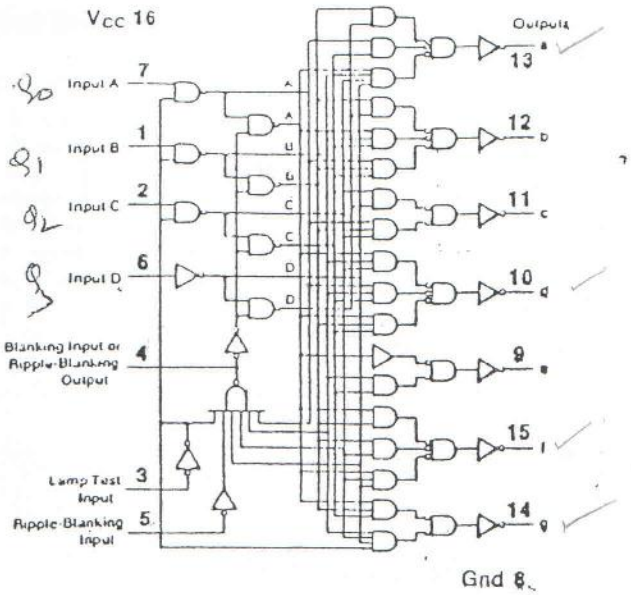
BCD-to-Decimal Decoder/Driver

54/7445 30V output rating
54/74145 15V output rating

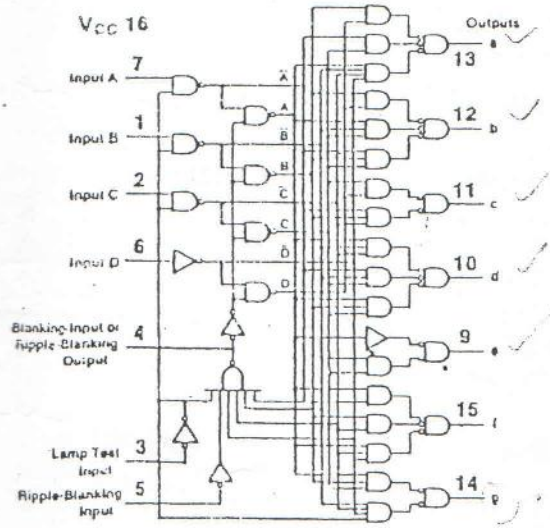


BCD-to-7-Segment Decoder/Driver

54/7446 30V/20mA output rating · 54/7447 15V/20mA output rating
54/7446A 30V/40mA output rating · 54/7447A 15V/40mA output rating

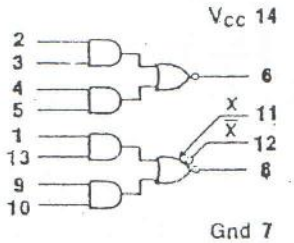


54/7448 BCD-to-7-Segment Decoder

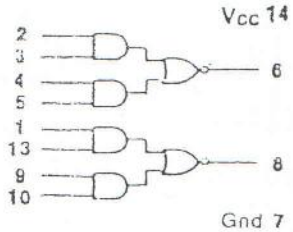


54/7450 Dual AND-OR-INVERT Gate

Expandable

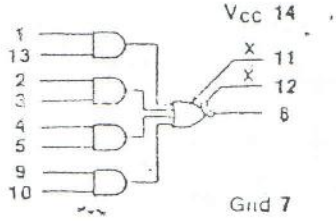


54/7451 Dual AND-OR-INVERT Gate

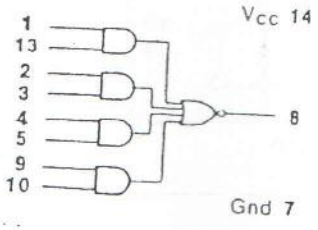


54/7453 Single AND-OR-INVERT Gate

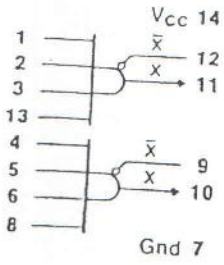
Expandable



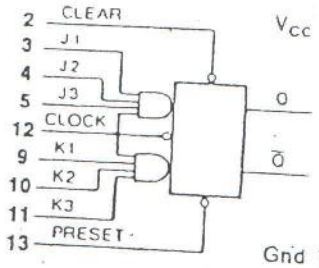
54/7454 Single AND-OR-INVERT Gate



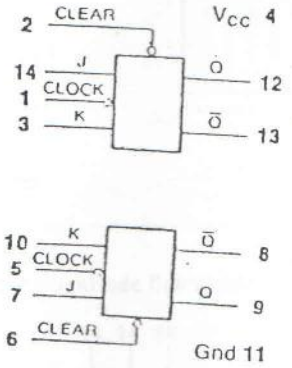
54/7460 Dual AND-OR Expander



54/7472 J-K Flip-Flop

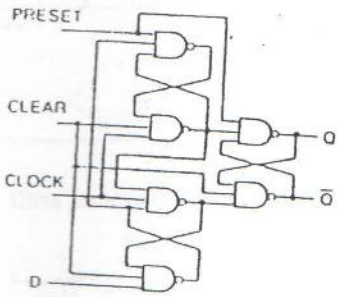


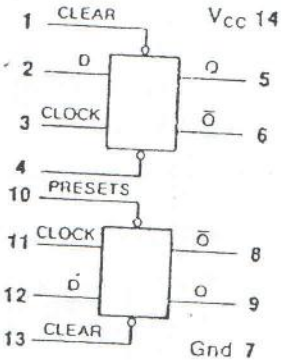
54/7473 Dual J-K Flip-Flop



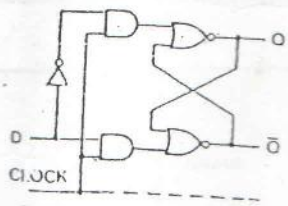
54/7474 Dual D Flip-Flop

D flip-flop logic





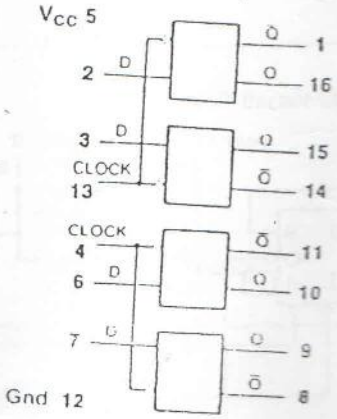
latch logic



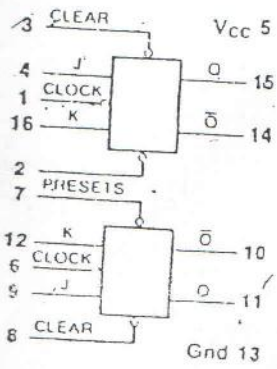
Truth Table

C	D	Q	$\bar{Q}$
Low	Low	No Change	
Low	High	No Change	
High	Low	Low	High
High	High	High	Low

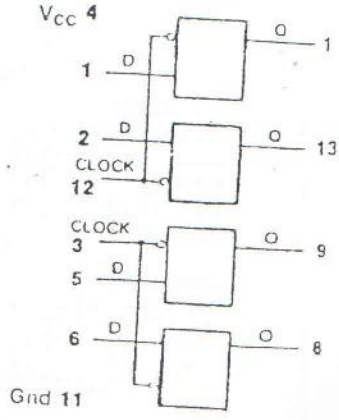
54/7475 Quad Latch



54/7476 Dual J-K Flip-Flop

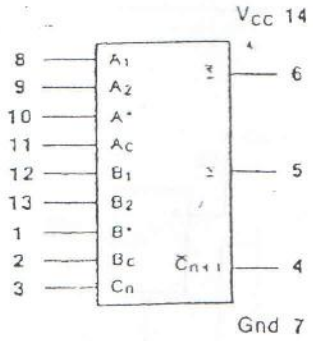


54/7477 Quad Latch



Refer to 54/7475 data

54/7480 Gated Full Adder

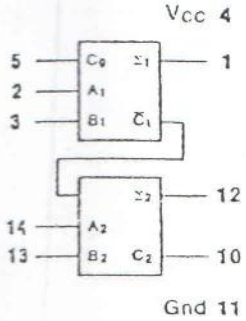


Truth Table

C_n	B	A	C_{n+1}	Σ	Σ
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

$A = A_1 \cdot A_2 + A_C$ $\quad A^* = \overline{A_1 \cdot A_2}$ $\quad B = B_1 \cdot B_2 + B_C$ $\quad B^* = \overline{B_1 \cdot B_2}$

54/7482 2-Bit Binary Full Adder



2-bit & 4-bit Adder Truth Table

ODD* bit positions:

INPUTS			OUTPUTS	
C_{x-1}	A_x	B_x	Σ_x	C_x
0	0	0	0	1
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	0

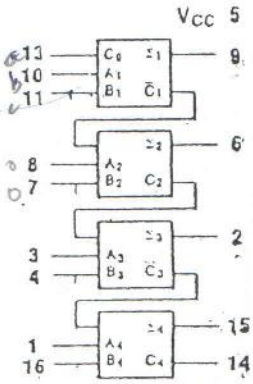
* X = 1 or 3

EVEN† bit positions:

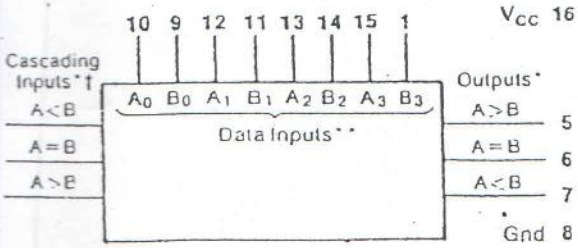
INPUTS			OUTPUTS	
C_{x-1}	A_x	B_x	Σ_x	C_x
1	0	0	0	0
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1

† X = 2 or 4

54/7483 4-Bit Binary Full Adder

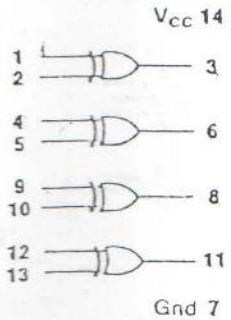


54/7485 4-Bit Magnitude Comparator

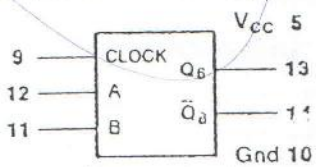


* a HIGH signal indicates a TRUE condition
† results from a comparison of lower-order bits
** inequality of these bits will override CASCADED inputs

54/7486 Quad Exclusive-OR Gate

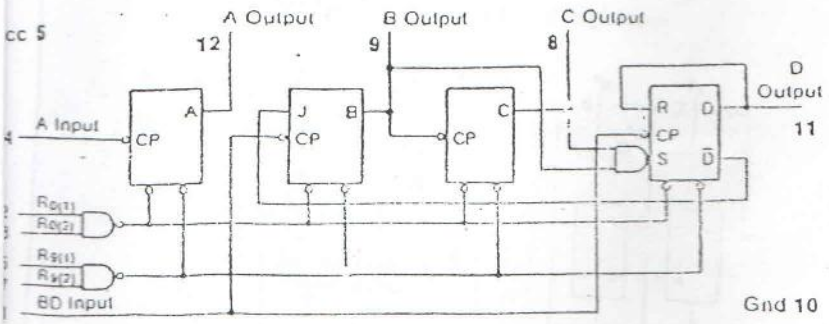


54/7491A 8-Bit Shift Register



Inputs at time t_n		Q output at time t_{n+d}
A	B	
0	0	0
0	1	0
1	0	0
1	1	1

54/7490 Decade Counter



Truth Tables

BCD Count Sequence*

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Reset/Count

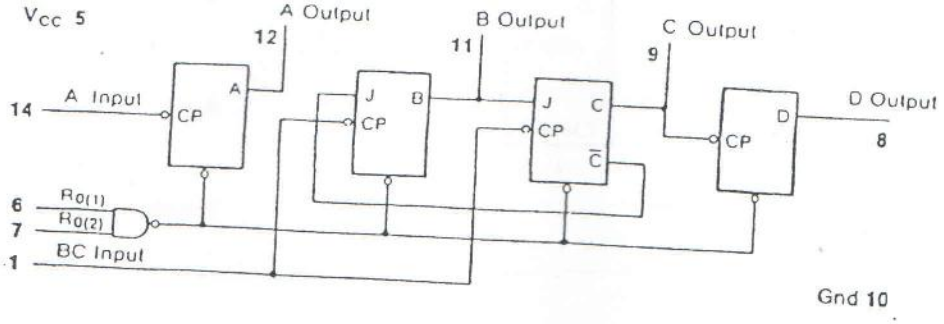
RESET INPUTS				COUNT
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	
1	1	0	↓	0 0 0 0
1	1	↓	0	0 0 0 0
↓	↓	1	1	1 0 0 1
↓	0	↓	0	Count
0	↓	0	↓	Count
0	↓	↓	0	Count
↓	0	0	↓	Count

* Output A connected to input BD ↓ = Immaterial

(7)

(71)

54/7492 Divide-by-Twelve Counter

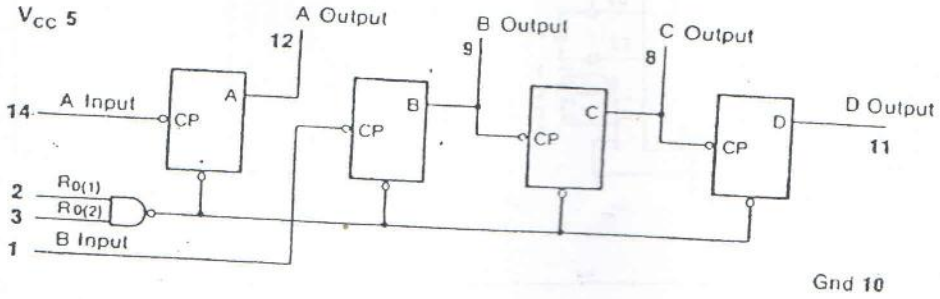


Truth Table

COUNT	OUTPUT		
	D	C	B
0	0	0	0
1	0	0	1
2	0	0	1
3	0	0	1
4	0	1	0
5	0	1	0
6	0	1	1
7	1	0	0
8	1	0	0
9	1	0	1
10	1	1	0
11	1	1	0

NOTE: Output A connected to

54/7493 Divide-by-Sixteen Counter

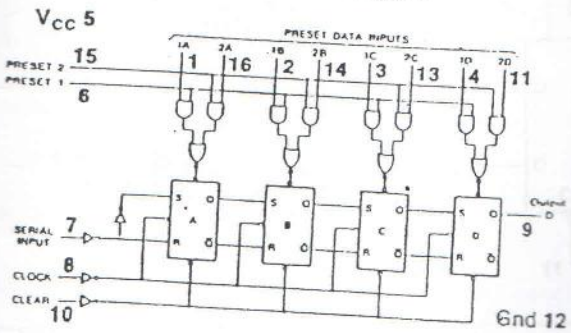


Truth Table

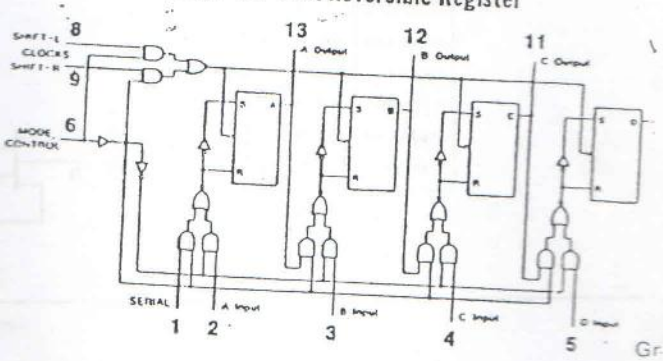
COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

NOTE: Output A connected to input

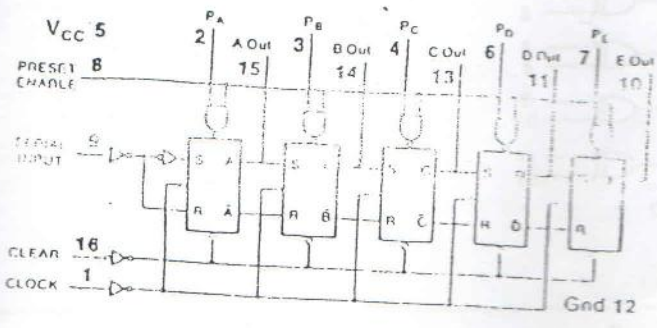
54/7494 4-Bit Shift Register



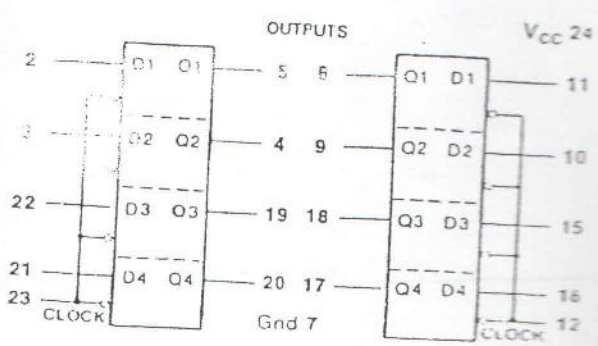
54/7495 4-Bit Reversible Register



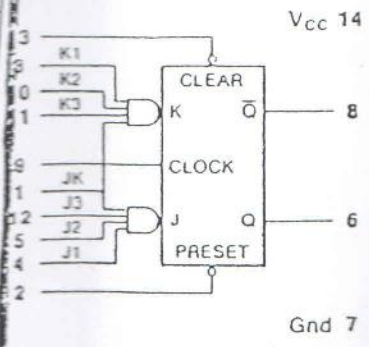
54/7496 5-Bit Serial/Parallel Register



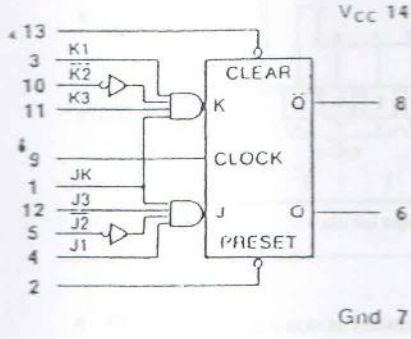
54/74100 8-Bit Bistable Latch*



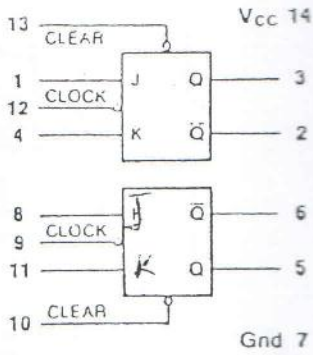
74104 Gated J-K Master-Slave Flip-Flop



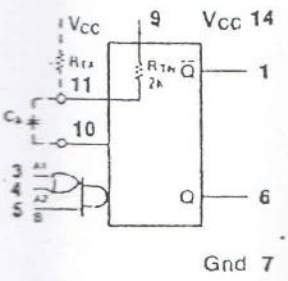
54/74105 Gated J-K Master-Slave Flip-Flop



54/74107 Dual J-K Flip-Flop



54/74121 Monostable Multivibrator

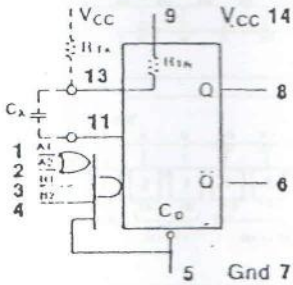


Triggering Truth Table

A1	A2	B	RESPONSE
↓	↓	↑	No Trigger
0	X	↑	No Trigger
X	0	↑	No Trigger
↓	0	X	No Trigger
↓	X	0	No Trigger
↓	↓	↑	Trigger
0	↓	X	No Trigger
X	↓	0	No Trigger
↓	↓	↑	Trigger

X = immaterial

54/74122 Retriggerable Multivibrator

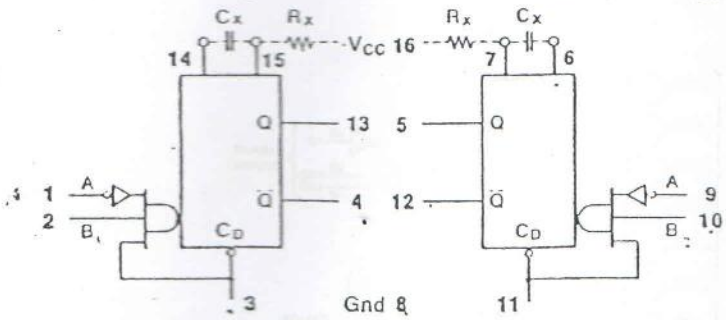


Triggering Truth Table

A1	A2	B1	B2	Cd	RESPONSE
X	X	X	X	0	No Trigger
↓	0	X	X	X	No Trigger
↓	X	0	X	X	No Trigger
↓	1	1	1	1	Trigger
X	X	↑	0	X	No Trigger
1	1	↑	X	X	No Trigger
0	X	↑	1	1	Trigger

*A1 & A2 are logically interchangeable, as are B1 & B2
X = immaterial

54/74123 Dual Retriggerable Multivibrator

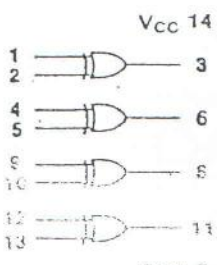


Triggering Truth Table

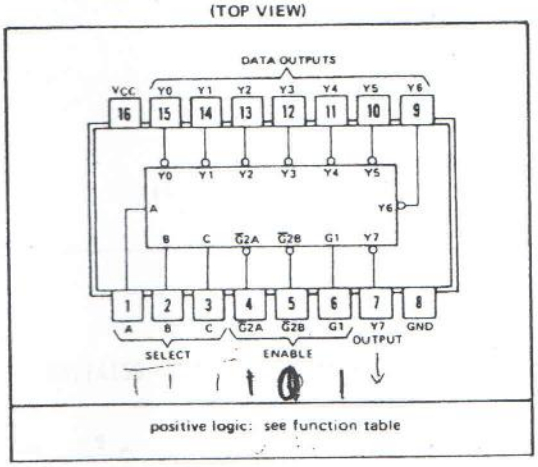
A	B	CD	RESPONSE
X	X	0	No Trigger
↓	0	X	No Trigger
↓	↑	1	Trigger
1	↓	X	No Trigger
0	↓	1	Trigger

X = immaterial

54/74136 Quad 2-input Exclusive-OR Gate

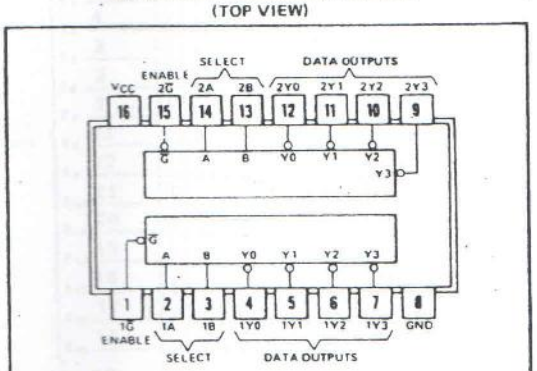


SN54LS138, SN54S138 . . . J OR W PACKAGE
SN74LS138, SN74S138 . . . J, N OR NS PACKAGE
(TOP VIEW)



positive logic: see function table

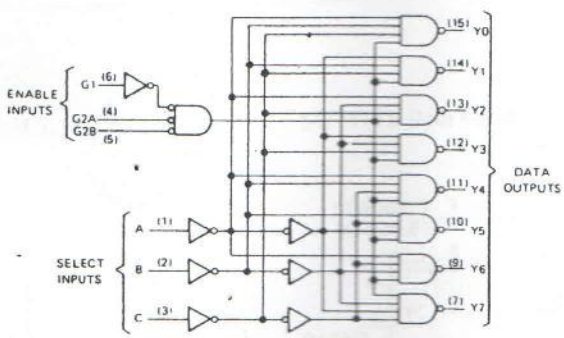
SN54LS139, SN54S139 . . . J OR W PACKAGE
SN74S139 . . . J OR N PACKAGE
SN74LS139 . . . J, N OR NS PACKAGE
(TOP VIEW)



positive logic: see function table

functional block diagrams and logic

'LS138, 'S138

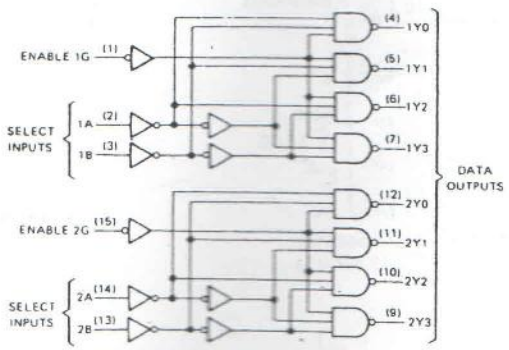


'LS138, 'S138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

$\overline{G2}$* = $\overline{G2A}$ + $\overline{G2B}$
H = high level, L = low level, X = irrelevant

'LS139, 'S139



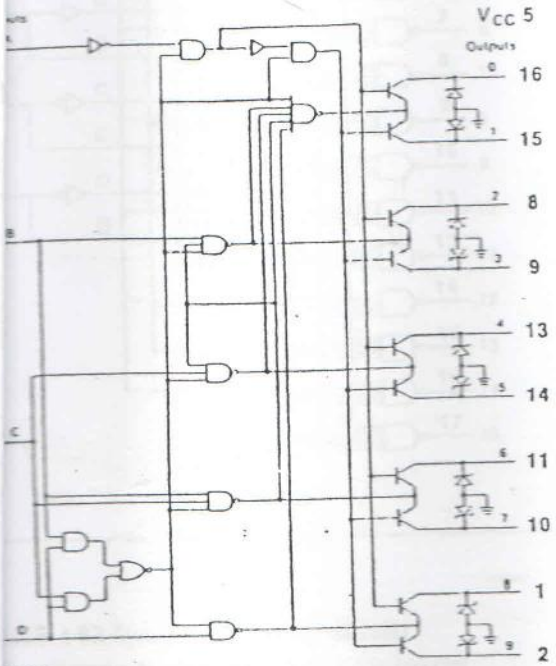
'LS139, 'S139
(EACH DECODER/DEMULTIPLEXER)
FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

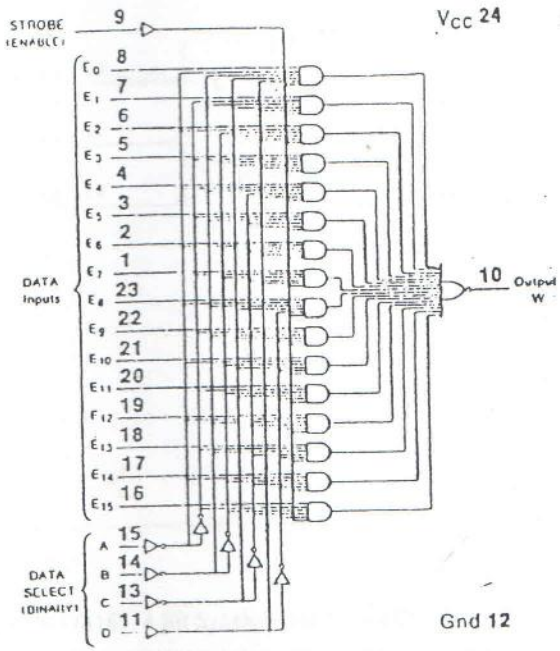
H = high level, L = low level, X = irrelevant

schematics of inputs and outputs

74141 BCD-to-Decimal Decoder/Driver

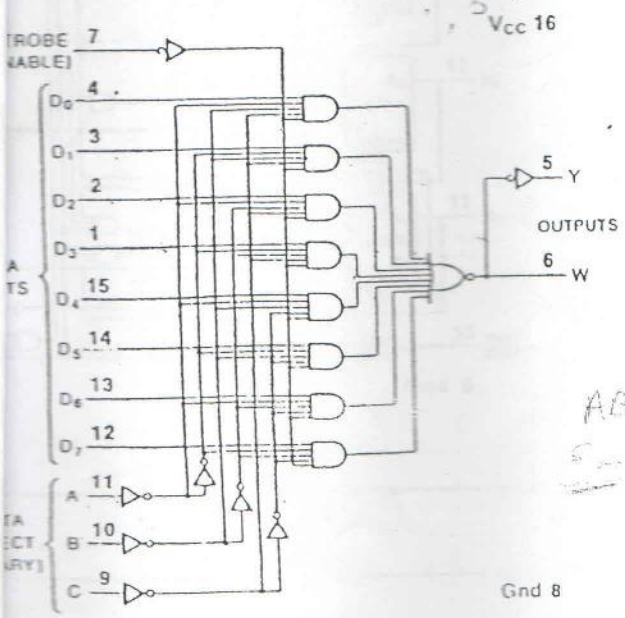


54/74150 16-Bit Data Selector/Multiplexer

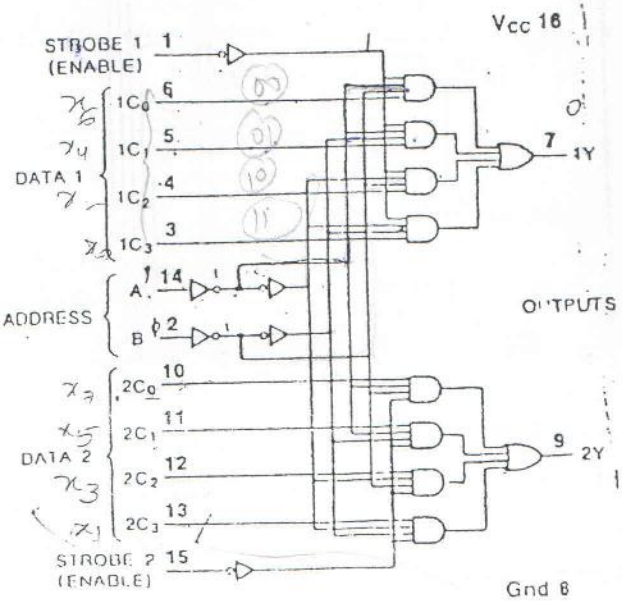


54145/74145 see page 5.

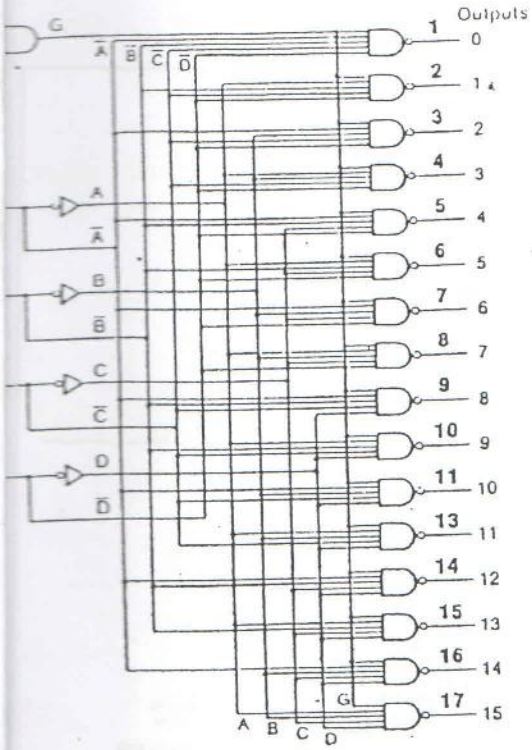
54/74151 8-Bit Data Selector/Multiplexer



54/74153 Dual 4-Line-to-1-Line Data Selector/Multiplexer



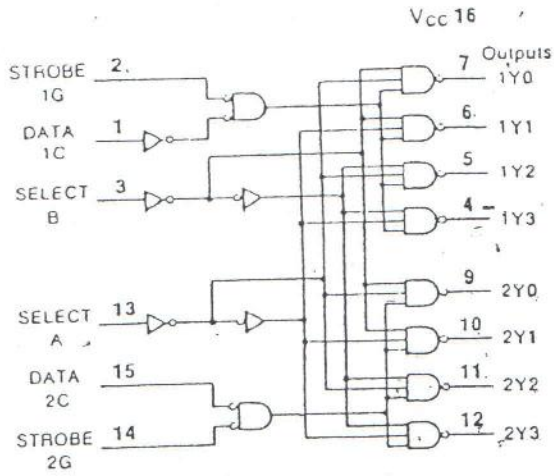
54 4-Line-to-16-Line Decoder/Demultiplexer



Dual 2-Line-to-4-Line Decoder/Demultiplexer

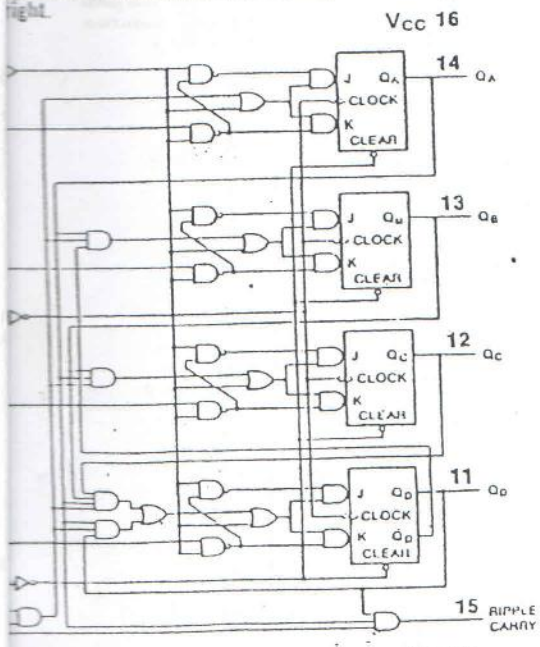
54/74155 Active pull-ups

54/74156 Free-collector outputs



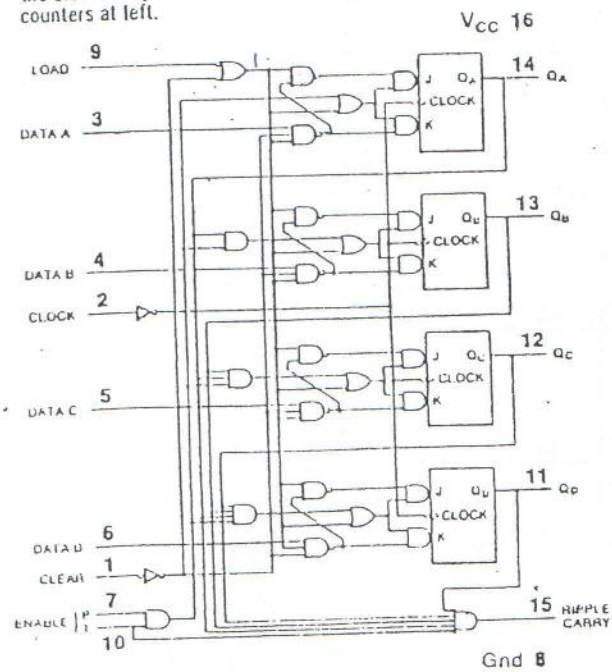
4160 4-Bit Synchronous Decade Counter

2 synchronous decade counters are similar; however synchronous as shown for the 54163/74163 binary right.

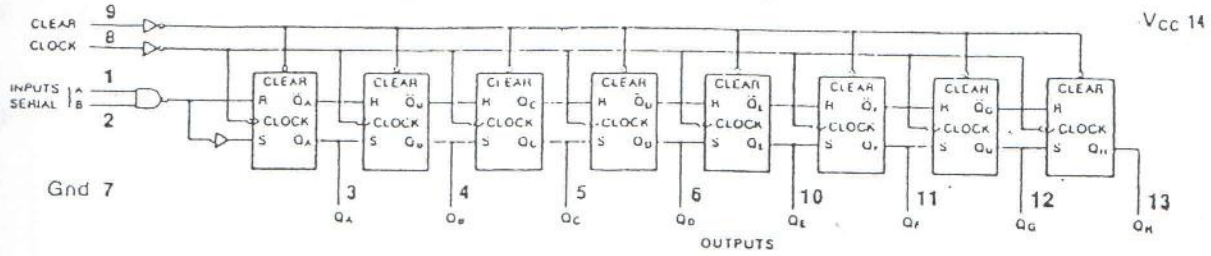


54/74163 4-Bit Synchronous Binary Counter

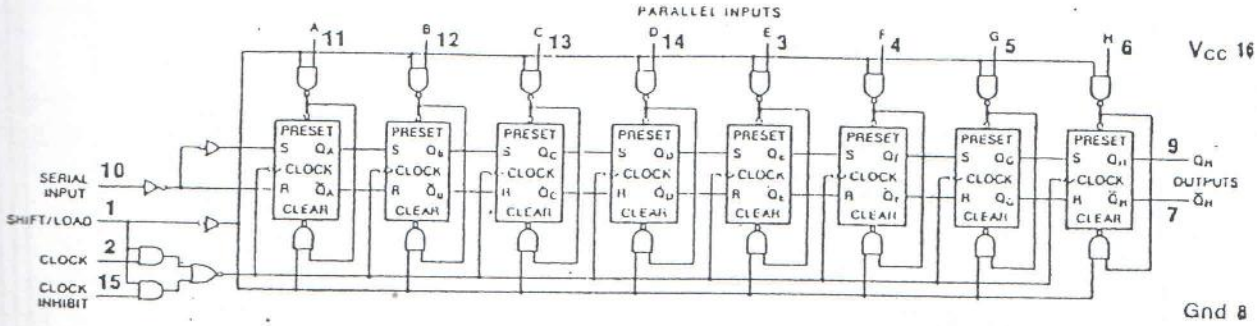
54161/74161 synchronous binary counters are similar; however the clear is asynchronous as shown for the 54160/74160 decade counters at left.



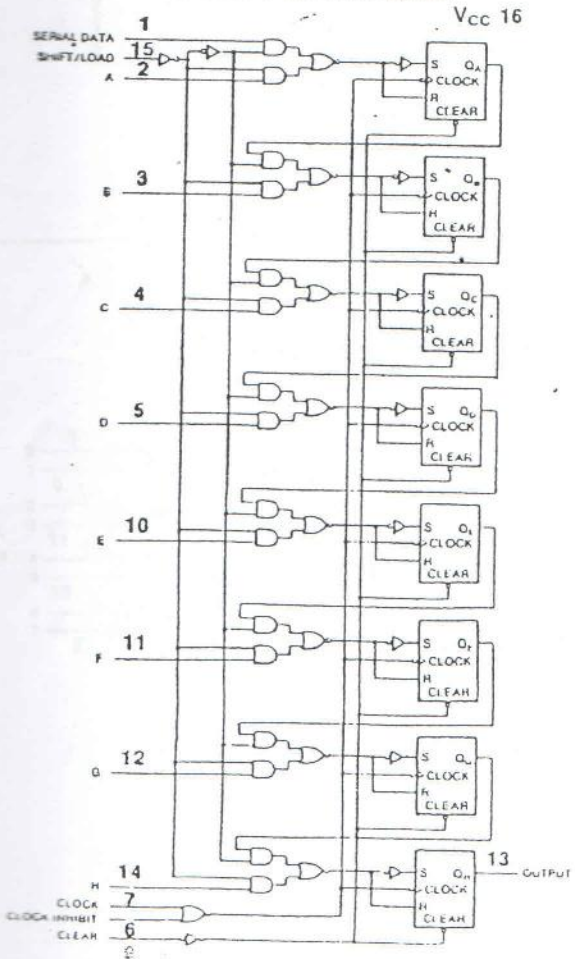
54/74164 8-Bit Parallel-Out Serial-Shift Register



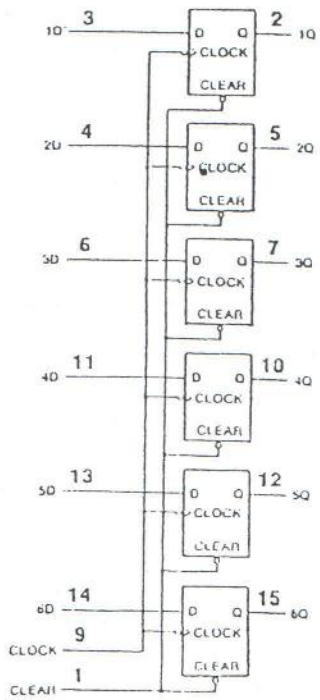
54/74165 Parallel-Load 8-Bit Shift Register



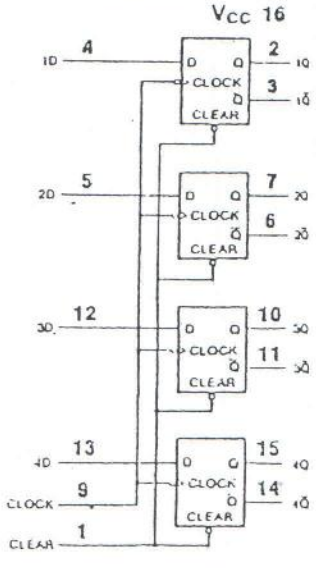
54/74166 8-Bit Shift Register



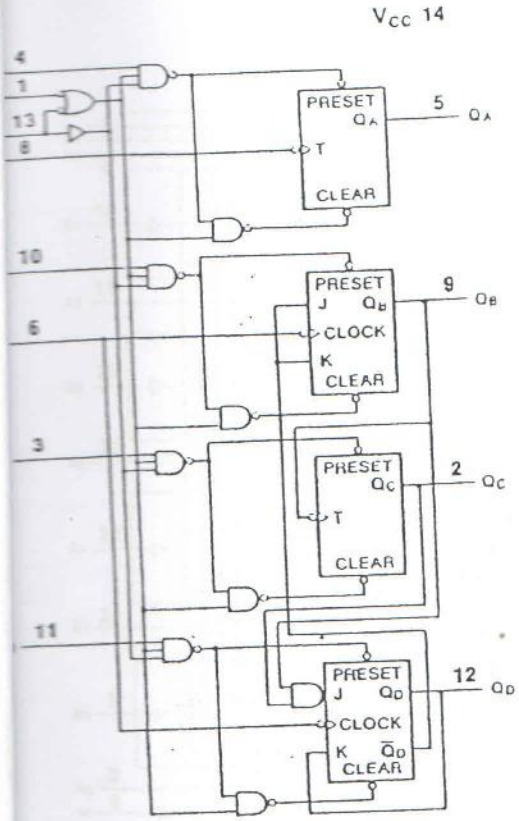
54/74174 Hex D-Type Flip-Flop



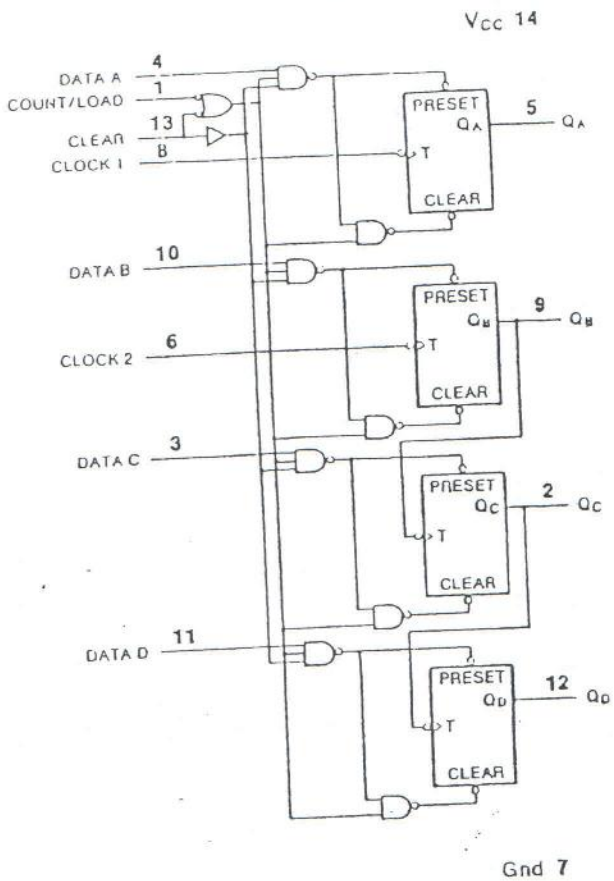
54/74175 Quad D-Type Flip-Flop



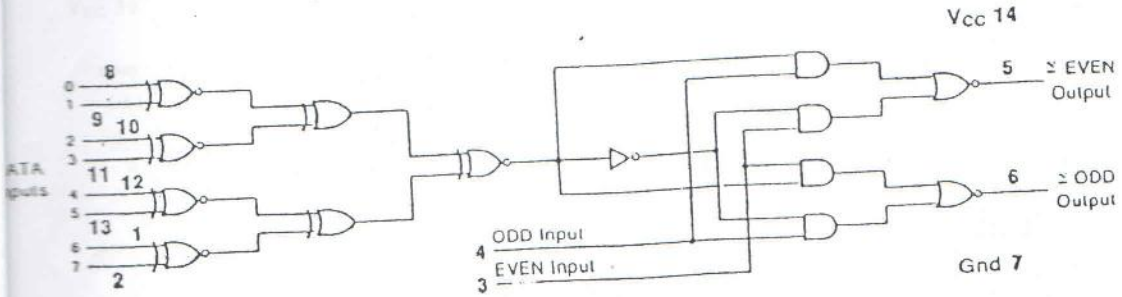
6 35 MHz Presettable Decade Counter/Latch



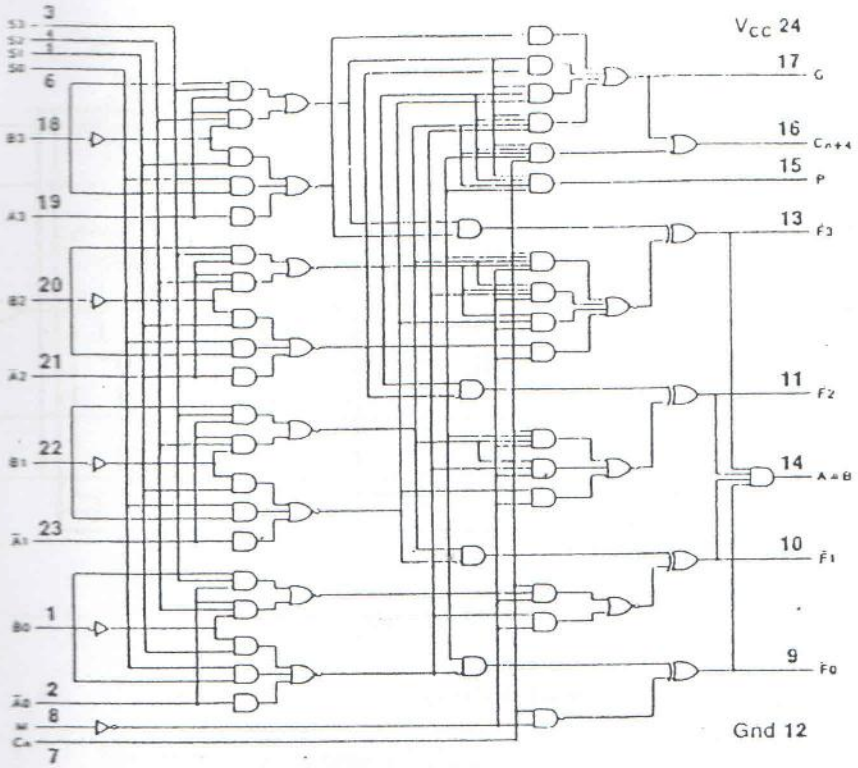
54/74177 35 MHz Presettable Binary Counter/Latch



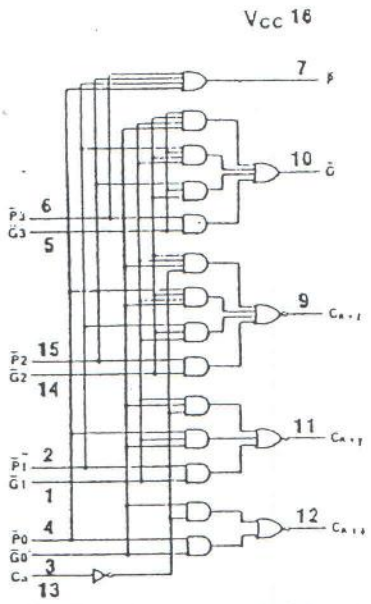
54/74180 8-Bit ODD/EVEN Parity Generator/Checker



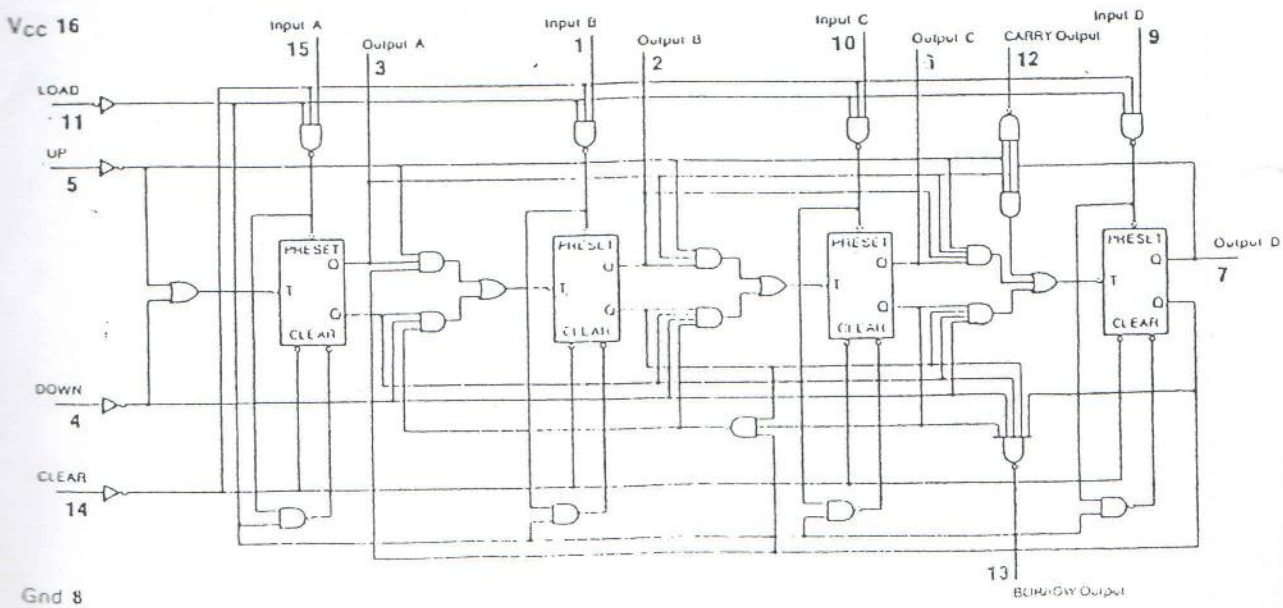
54/74181 4-Bit Arithmetic Logic Unit



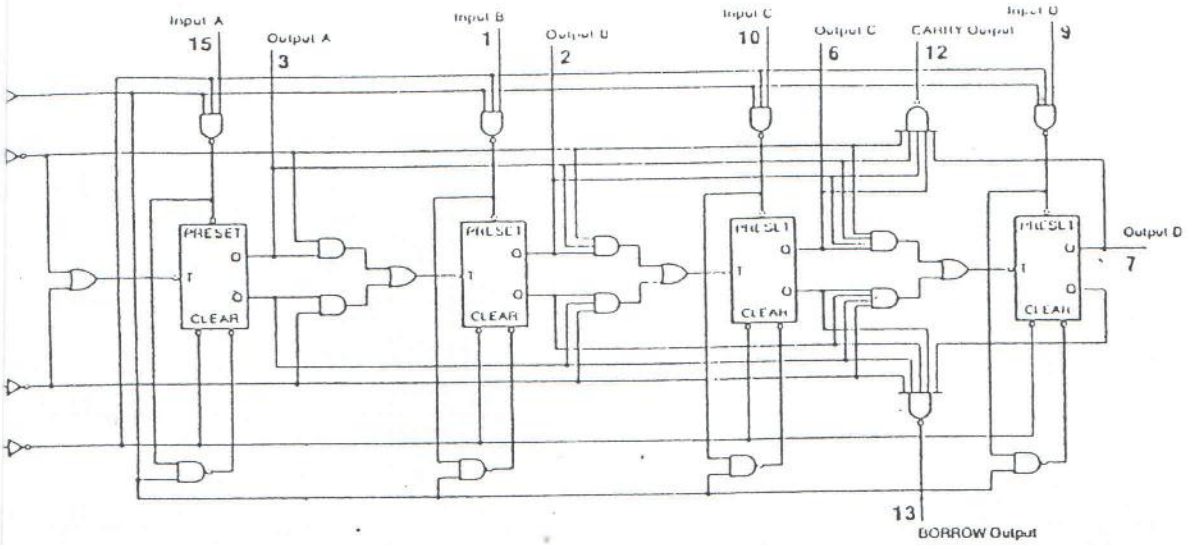
54/74182 Look-Ahead Carry Generator



54/74192 Reversible BCD Decade Counter



54/74193 Reversible Modulo-16 Binary Counter

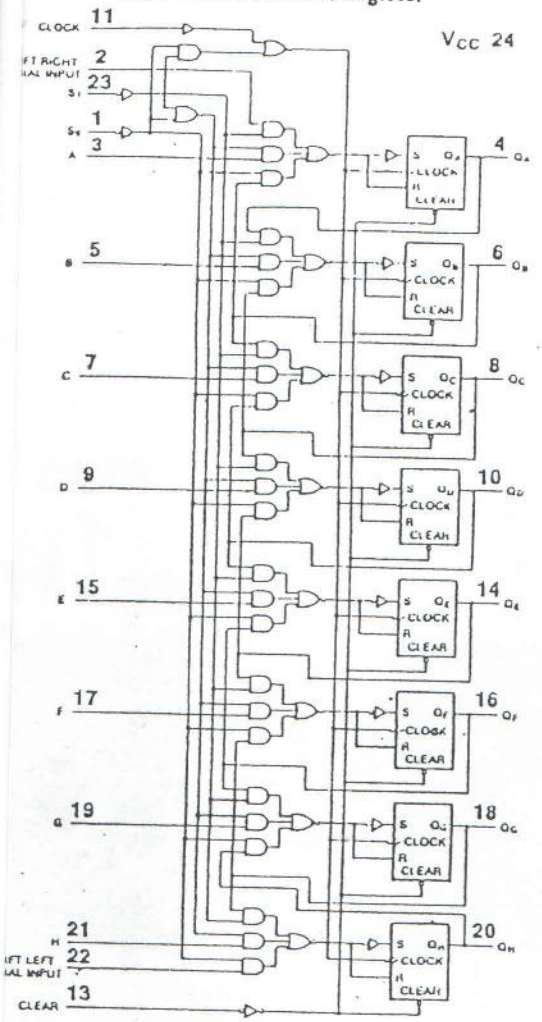


Operations Table

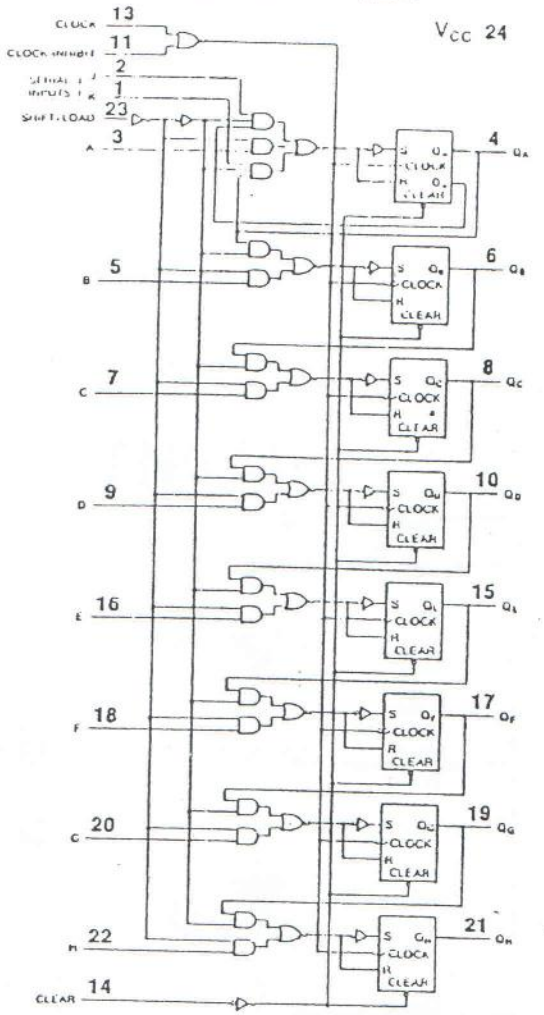
OPERATION	INPUTS					RESPONSE AT Q OUTPUTS
	UP CLOCK	DOWN CLOCK	CLEAR	LOAD	A, B, C, D	
Clocking	⎍	1	0	1	X	Count UP
	1	⎍	0	1	X	Count DOWN
	0	⎍	0	1	X	Q_A unchanged; others unchanged if Q_A is high
	⎍	0	0	1	X	Q_A unchanged; others unchanged if Q_A is low
	⎍	⎍	0	1	X	Undefined for race conditions
Clearing	↓	↓	1	X	X	All 0's
Loading	1	1	0	1	X	No change
	↓	↓	0	0	PRESET DATA	Preset to A, B, C, D input data

X = irrelevant ↓ = high level recommended

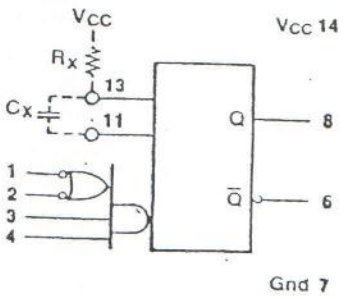
54/74198 8-Bit Shift Register



54/74199 8-Bit Shift Register



9601 Retriggerable One-Shot

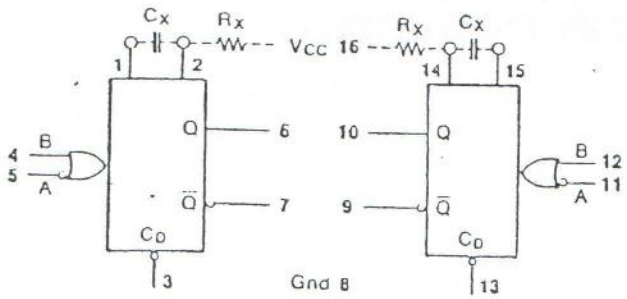


Triggering Truth Table

Pin 1	Pin 2	Pin 3	Pin 4	RESPONSE
High	High	↓	↑	No Trigger
Low	↑	↓	High	Trigger
Low	↑	↓	Low	No Trigger
↑	High	High	High	Trigger
↑	High	Low	↑	No Trigger
↑	Low	↑	↑	No Trigger

↑ = unmaterial

9602 Dual Retriggerable One-Shot



Triggering Truth Table

A	B	C_D	RESPONSE
X	X	0	No Trigger
↓	0	X	No Trigger
↓	1	1	Trigger
1	↓	X	No Trigger
0	↓	1	Trigger

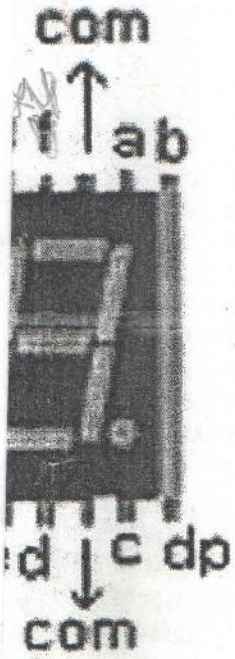
X = unmaterial

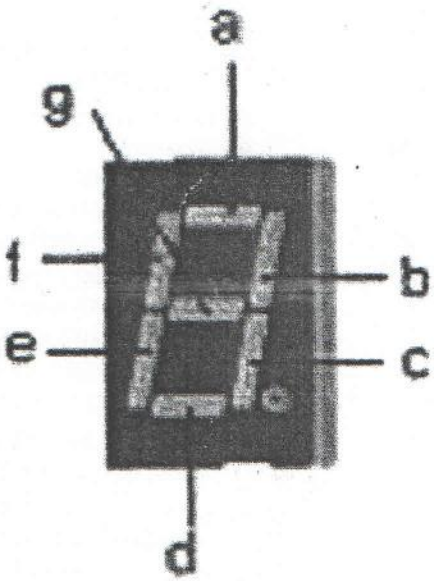
TEMPERATURE RANGE
MILITARY INDUSTRIAL

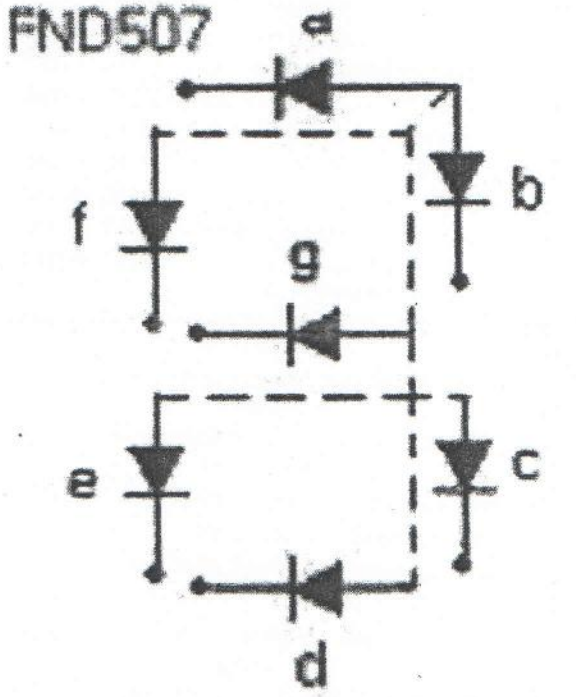
705-1*	705-2*
706-1*	706-2*
708-1*	708-2*
709-1*	709-2*
727-1	727-2
728-1	727-2
729-1	729-2
736-1	736-2
737-1	737-2
744-1	744-2
751-1	751-2
770-1	770-2
771-1	771-2
772-1	772-2
773-1	773-2
774-1	774-2
775-1	775-2
776-1	776-2
777-1	777-2
778-1	778-2
779-1	779-2
—	781-2

930-1	930-2
932-1	932-2
933-1	933-2
936-1	936-2

*705=9093;



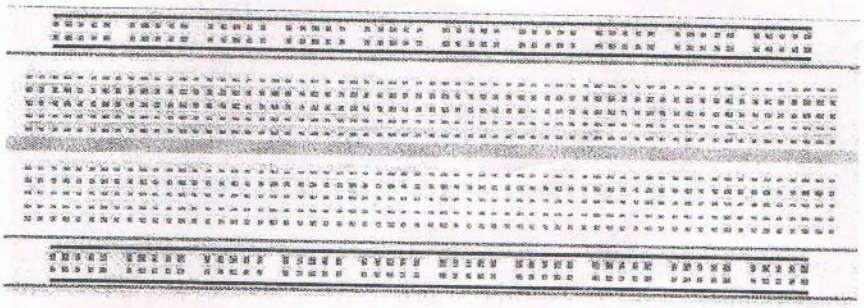




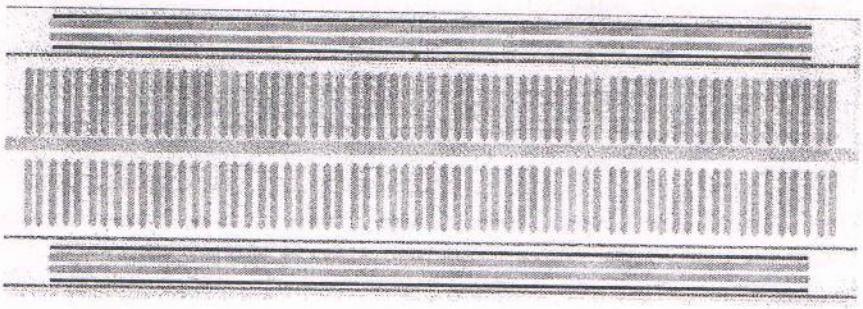
<Common Anode>

What is a breadboard?

A breadboard is used to build and test circuits quickly before finalizing any circuit design. The breadboard has many holes into which circuit components like ICs and resistors can be inserted. A typical breadboard is shown below:



The bread board has strips of metal which run underneath the board and connect the holes on the top of the board. The metal strips are laid out as shown below. Note that the top and bottom rows of holes are connected horizontally while the remaining holes are connected vertically.



To use the bread board, the legs of components are placed in the holes. Each set of holes connected by a metal strip underneath forms a *node*. A node is a point in a circuit where two components are connected. Connections between different components are formed by putting their legs in a common node.

The long top and bottom row of holes are usually used for power supply connections. The rest of the circuit is built by placing components and connecting them together with jumper wires. ICs are placed in the middle of the board so that half of the legs are on one side of the middle line and half on the other.

A completed circuit might look like the following.